4.5 Working Group 10.5 (Design and Engineering of Electronic Systems)

The Working Group 10.5 "Design and Engineering of Electronic Systems" belongs to the IFIP Technical Committee 10, and was established in 1994. The WG 10.5 home-page is located at http://www.inf.ufrgs.br/ifip10-5. The main activity of the Working Group is in the frame of the International Conference on Very Large Scale Integration, IFIP-VLSI-SoC.

4.5.1 Members

The following persons became members of WG 10.5 in October 2009: Matthew Guthaus , Ian O'Connor, and Chi Ying Tsui

- **Matthew Guthaus**, UC Santa Cruz, USA
Matthew Guthaus is Assistant Professor at Computer Engineering of University of California Santa Cruz, California. He is very active and he is willing to propose the organization of VLSI-SoC2012 in Santa Cruz California. *Topics : VLSI Design Automation for reliability and variability*

- **Ian O'Connor**, Ecole Centrale de Lyon, France
Ian O'Connor is Professor for Heterogeneous and Nanoelectronics Systems Design at Ecole Centrale de Lyon, France. He is currently head of the Heterogeneous Systems Design group at the Lyon Institute of Nanotechnology (approximately 200 people), of which he is also one of the deputy-directors. Since 2008, he also holds a position of Adjunct Professor at Ecole Polytechnique de Montréal, Canada. *Topics: Design, emerging technologies, nanoscale computing fabric, Optical Noc's*

- **Chi Ying Tsui,** Dept. of Electr. & Comp. Eng. HK S&T, China (over skype conference)
Pr. Tsui (Chi Ying) from Hong Kong, working on VLSI design. He offers to organize VLSI-SoC in 2011 in Hong Kong, and is very active in the research fields of low power circuit and system design. He was the Chair of Low Power Design sub-committee of ACM-SIGDA Technical Committee in 2006 and currently a member of the sub-committee. He is also serving on the editorial board of Integration, the international VLSI Journal. He helped in organizing the ASP-DAC conference and served on the technical programming committee in many other international conferences and symposium.
Topics : Low Power Design : Digital, Wireless Baseband System, SoC and Network-on-chip design; Power Management System Design for DVFS.

As a result, as of today the working group has 65 members. Their geographic distribution is as follows: North America – 17, Europe – 36, Asia / Pacific – 10, South America – 2

4.5.2 Officers

The officers of WG 10.5 are:

- Prof. Michel Robert (France), Working Group chair
- Prof. Ricardo Reis (Brazil) and Luis Miguel Silveira (Portugal), Vice-chairs
- Prof. Flavio Wagner (Brazil), Past chair

4.5.3 Meetings

The following business meetings were conducted by WG 10.5 during the last 12 months:

- Nice, France, April 20, 2009, during DATE conference
- San Francisco, July 31, 2009, during DAC conference
- Florianopolis, Brazil, on October 12, 2009, during VLSI-SoC 2009
- Dresden, on March 9, 2010,Germany during the DATE conference in 2010.

Our next IFIP WG 10.5 workgroup meeting will be organized during VLSI-SOC 2010 in Madrid Tuesday, september 28 th, from 6. PM to 8. PM.

4.5.4 Sponsored Events : http://www.vlsi-soc.com/

The 17th IFIP International Conference on Very Large Scale Integration (VLSI-SoC) was held in Florianopolis, Brazil, from October 12 to 15, 2009.
The General Chair, was Pr. Ricardo Reis (Porto Alegre), and the Program Chair Pr. Jürgen Becker (Karlsruhe), members of the WG 10.5. 29 full papers (+ posters) out of 81 submitted. About 100 participants registered.
Springer will produce the book of the best contributions extracted from the IFIP-VLSI-SoC' conferences (best papers + feedback of the presentation).

EduTech was also organized in Florianopolis, together with VLSI-SoC, in 2009 (October 15, 16), but was not successful (only 30 attendees).

4.5.6 Planned Events

The following main sponsored events are already planned:

- **IFIP-VLSI-SoC'10** – 18th International Conference on Very Large Scale Integration, will be held in Madrid, Spain from September 28 to 30, 2010
- General Chair : Pr. David Atienza, EPFL Lausane, member of the WG 10.5
- Keynotes are fixed. Subhasish Mitra (Stanford), Giovanni de Micheli (EPFL), Sani Nassif (IBM), Nik Dutt (UC Irvine)
- **Conference special theme: Green computing**
- Two special sessions: 1- Green computing and datacenters, 2- Bioengineering VLSI
-Sponsoring: IFIP 50%, CEDA 25%, CASS 25%
- Target attendance : 100
- U. Madrid - provides auditorium + 3 meeting rooms

- **IFIP-VLSI-SoC'11**
- General Chair : Pr, Chi-Ying Tsui**,** member of the WG 10.5
- Proposal 17-19 October
- Theme suggestion for conference "SOC design for ubiquitous sensing and computing". To be discussed taking into account TC10 priorities (green electronics).

- **IFIP-VLSI-SoC'12 (Santa Cruz)**
Target 7th or 14th October (avoid last week in September (classes start and hotels expensive)
- Target attendance : 120-on-site + 50 off-site from Silicon Valley

4.5.7 Special Interest Groups
The "green computing" topic will be discussed during our next meeting and conference in Madrid where a specific session will be organized.