IFIP Working Group 10.5 Minute Meeting

October 12, 2025 5pm-6:30 pm

Puerto Varas (Chile) @VLSI-SOC 2025

Notes taken by Graziano Pravadelli

Attendees in presence: Giovanni De Micheli, Victor Grimblatt, Graziano Pravadelli, Ricardo Reis

Attendees in remote mode: Tiziana Margaria, Yuanqing Cheng, Florenc Demrozi, Fatih Ugurdag, Yue Zhang (invited to present candidature for organizing VLSI-SOC in 2027 in Bejing)

Apologies: Luc Claesen, Luis Miguel Silveira, Leticia Bolzani Phoehls, Salvador Mir, Katell Morin Allory, Matteo Sonza Reorda, Nicola Bombieri, Samuele Germiniani, Abe Elfadel, Matthew Guthaus, Ian O'Connor

Agenda

- Communications
- Status of VLSI-SOC 2026
- Proposal for organizing VLSI-SOC 2027
- Report of VLSI-SOC 2025

1. Communication

The chair remembers the rules to be part of the WG 10.5:

- Attending WG 10.5 meetings, participating in the TPC of VLSI-SOC or the conference itself, submitting papers
- After two years of inactivity the WG chair will reach out via email to assess interest and availability to continue as part of the WG

The rules are operative from October 2024, thus at the end of the next year people that were not involved as reported above will be contacted to understand if they are still interested in being part of the WG.

The chair informs that Prof. Demorosi has completed the setup of the VLSI-SOC series of events. From 2026 the current year event will be available at https://www.vlsi-soc.com which will be redirected to https://vlsi-soc.github.io/vlsi-soc/

Past year event will be moved to https://vlsi-soc.github.io/vlsi-soc/202X/ and linked to the main site in the past event page.

The chair informs he completed on June, the submission of VLSI-SOC documentation for the ICORE ranking (https://www.core.edu.au) asking for the class B. Decision is expected in 2026.

The chair informs about two initiatives derived from the mapping of competences:

Submission of a COST action proposal, titled "**Hardware-Aware AI Architectures for Scalable and Interpretable Genome-Wide Regulatory Modeling**", to finance the organization of workshops, schools, meetings among international researchers.
The proposal has been coordinated by prof. Rosalba Giugno (UNIVR) that asked to identify people with expertise in AI-aware architecture design and optimization. The following WG 10.5 members have been then involved: N. Bombieri, L. Bolzani Phoelps, F. Demrozi, S. Germiniani, G. Pravadelli, L.M. Silveira, F. Ugurdag, Ozyegin University, Turkey, E.I, Vatajelu. If funded furthere people can be invited to participate.

Organization of the Advanced School on AI and Intelligent Systems (AIS) 2025, supported by IEEE CEDA, IEEE CAS, Synopsys, University of Verona, and Municipality of Favignana, with the contribution from the following members of the WG: N.Bombieri, G. Pravadelli, M. Sonza Reorda, Y. Cheng, I. O'Connor and A. Elfadel.
The school was in Favignana (Italy) from September 1 to September 5. There were 24 participants 11 PhD students, 12 university faculties, 1 from industry. It included 3 lectures from M. Sonza Reorda (Politecnico di Torino, IT), Y. Zoriant (Synopsys, USA), Abe Elfadel (Khalifa University, UAE), and 6 tutorials organized by Y. Chen.
Next year the school will be host again in Favignana to amortise 2025 effort and consolidate the school organization. The date will be anticipated to June 8-12, which seems a better period for maximizing participation of PhD students.
Three lectures have been already confirmed their presence (Giovanni De Micheli, EFL, Ian O'Connor, ECPL, and Elham Azizi, Columbia University). WG members can contribute with tutorials and participating.
Prof. Reis suggested to involve AMC SIGDA for supporting the school.
Dr. Grimblatt suggested to move the school outside Italy, to promote the international visibility and participation.

2. Status of VLSI-SOC 2026

Prof. Margaria and prof. Demrozi presented the status of the organization for 2026. The conference will be in Limassol, Cyprus, from October 11 (tutorial day) to 14 at the St. Raphael hotel.
Organizers expect between 100 and 120 participants.

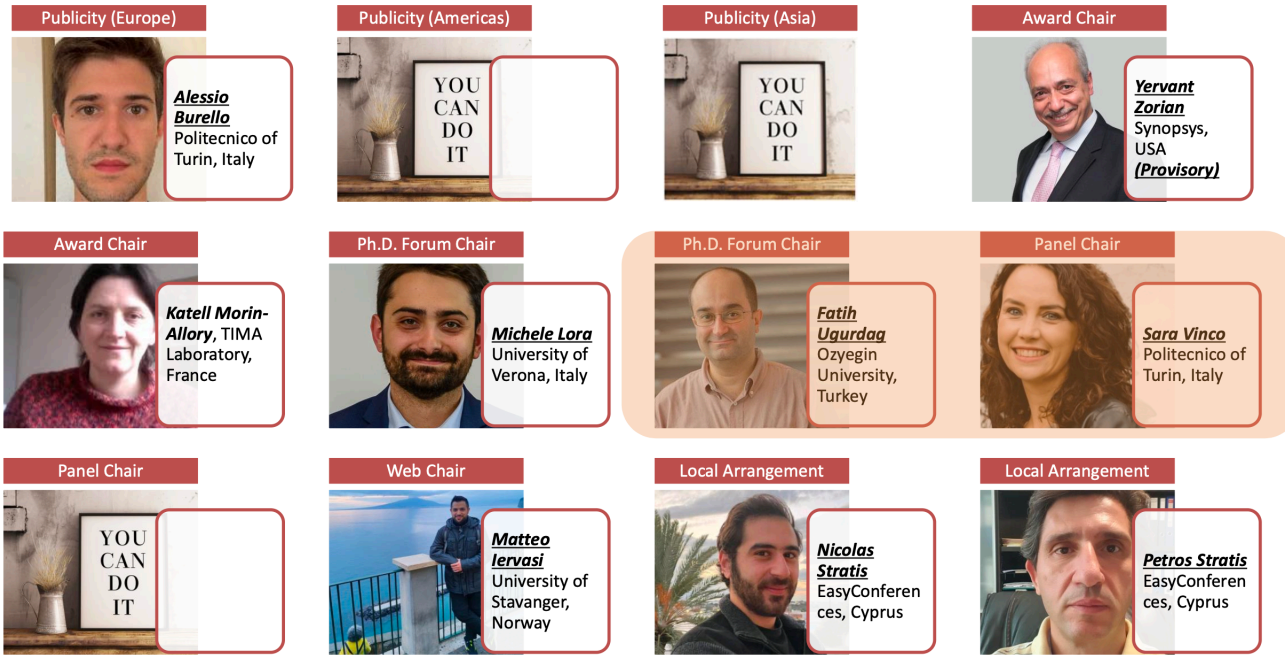
Registration fees are the same as this year (Euros instead of USD):

- Full registration (members): 600 Euros
- Full registration (non-members): 750 Euros
- IEEE life members: 250 Euros
- Students (members): 250 Euros
- Students (non-members): 300 Euros

Key dates are:

- Abstract: April 28
- Full paper: May 5
- Notification: June 16
- Camera ready: July 7

The status of the organizing committee is as follows:



The hotel is booked, and the web site will be visible in the coming days right after the end of VLSI-SOC 2025.

The chair remembered to include the ACM journal special issue in the call for paper and to not extend the submission deadline more than 1 week after May, with a strong involvement of WG members to promote paper submission.

Prof. Reis suggested for the future edition to anticipate the submission of the conference for the IEEE CAS and CEDA approval such that the event can be made public in the IEEE calendar.

3. Proposal for the organization of VLSI-SOC 2027 in China

Prof. Yue Zhang and prof. Y. Cheng from the Beihang University presented a proposal to organize VLSI-SOC 2027 in Bejing from Oct. 10 to 13.

Prof. Zhang identifies two possible alternatives for the conference hotel:

- Shangri-la Hotel Beijing
- Park Plaza Beijing Science Park

Plenty of slides were presented to show city and hotel facilities.

He is expecting of having a large participation (300 people) and he presented a budget accordingly.

He finally reported a proposal of the organizing committee where he will act as general chair, prof. Amara Amara as general co-chair, prof. Cheng as local chair, Dr. Zoriant as program chair and Prof. Yongpan Liu and prof. Prof. Sorin Cotofana as program co-chairs.

The proposal is solid and well presented.

The chair remembered that at least one between the general co-chair and the program co-chair should be from the steering committee.
He also remembered it is important to organize a social event on the Tuesday afternoon which includes a tour to appreciate the local culture.

We then discussed the need of anticipating the conference to the first week of October as tradition and required by CEDA to avoid conflict with other IEEE initiatives, but Prof. Zhang remembered that the first week of October is holiday in China.
Prof. De Micheli agrees on the fact that it is not advantageous having the conference during Chinese holidays.

A decision will be taken from the steering committee during the meeting scheduled on Oct 14 and the proposers will be informed accordingly.

4. Report from VLSI-SOC 2025

Victor Grimblatt reports that the number of participants is 57 persons with 44 submissions and 29 accepted papers + 2 special sessions (7 papers) + 1 panel + 2 tutorials.
He expresses his disappointment about the weak involvement of WG members with a few paper submissions and participation in presence limited to 4 members.
He informs the WG that this year the conference balance is negative, and he is going to cover the expenses by himself.
He suggests having a mandatory rule about the fact that at least one representative of the next year organizing committee is present at the current event.

Next meeting: at DATE 2026.