IFIP Working Group 10.5 Minute Meeting

October 6, 2024 4pm-6pm

Tangier(Morocco) @VLSI-SOC 2024

Notes taken by Graziano Pravadelli

Attendees in presence: Graziano Pravadelli, Salvador Mir, Ricardo Reis, Luis Miguel Silveira, Ioana-Elena Vataljelu, Said Hamdioui, Fatih Ugurdag
Attendees in remote mode: Katell Morin-allory, Ibrahim Elfadel, Florenc Demrozi, Andrea Calimera, Luc Claesen

Apologies: Donatella Sciuto, Matthew Guthaus, Lutfi Albasha, Jurgen Becker, Chi Ying Tsui, Manfred Glesner, Michael Hubner, Giovanni De Micheli

Agenda

- Communications
- Mapping of competences
- Status of VLSI-SOC 2024
- Status of VLSI-SOC 2025
- Status of VLSI-SOC 2026
- Any other business

1. Communication

Graziano remembers the possibility of publishing contributions related to WG 10.5 activities in the IFIP Insights issues, which appear monthly. Next deadlines are:

- October 22
- November 22
- December 22

To contribute send to Graziano the tile and a short description (~200-500 words) of the activity/event to be published before the deadlines.
For the October issue, Said and Iona will report on VLSI-SOC 2024.

2. Mapping of WG competences

Graziano announces the mapping of WG competences is finally completed and the results are published on the WG 10.5 web site.

A final set of 12 topics and 38 subtopics have been selected starting from a matrix composed of 46 topics and 40 application fields.
The selected topics are:

- AI architectures and applications
- Analog, digital and mixed-signal circuits design and syntesis
- Communication architectures and technologies
- Computing paradigms
- Embedded system design
- Emerging technologies and applications
- Smart systems, devices and applications
- Low-power, energy-efficient and thermal-aware design
- Security
- Sensors and signal processing
- System specification, simulation and verification
- Test and dependability

Per each topic, two topics leaders have been defined. The descriptions of the topics have been written and 29 members have participated in the mapping.

Topics	# members
Applications and Architectures for AI and ML	11
Digital circuits design and synthesis	8
Communication architectures and technologies	4
Computing paradigms	6
Embedded system design	8
Emerging technologies and applications	10
Smart systems, devices and applications	10
Low-power, energy-efficient and thermal-aware design	6
Security	3
Sensing and signal processing technologies	4
System specification, simulation and verification	5
Test and dependability	5

The mapping has been published on the WG web site: https://cisd.di.univr.it/wg10-5/competences.html

To better align with the mission of the WG, we should also consider organizing Project Partner "Matching" events during the conferences.

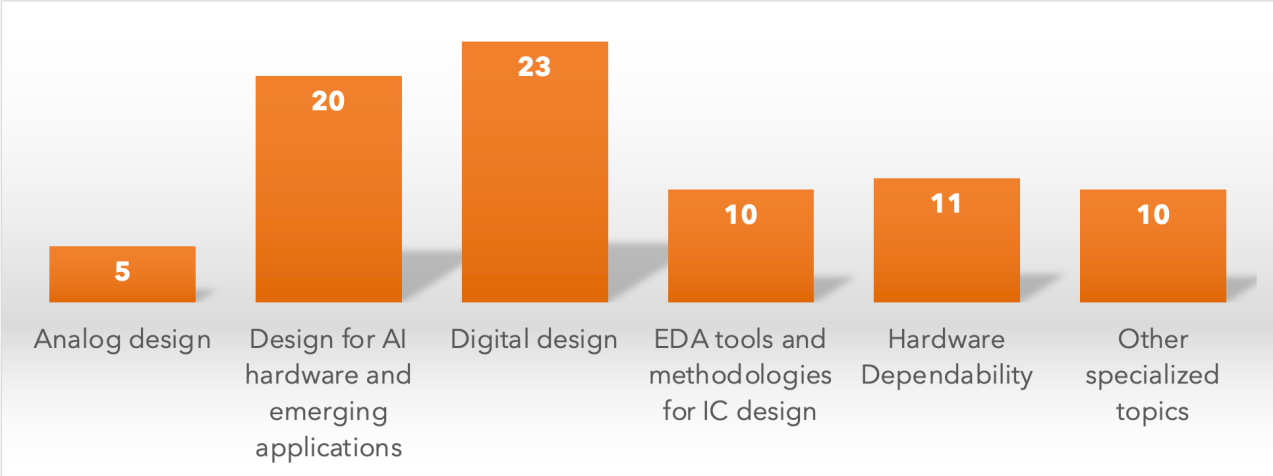
For example, VLSI-SoC typically coincides with the release of EU calls, as well as many national calls. Organizing these types of sessions during WG-sponsored events could be very beneficial in this context. Other conferences are already doing this.

3. Status of VLSI-SOC 2024

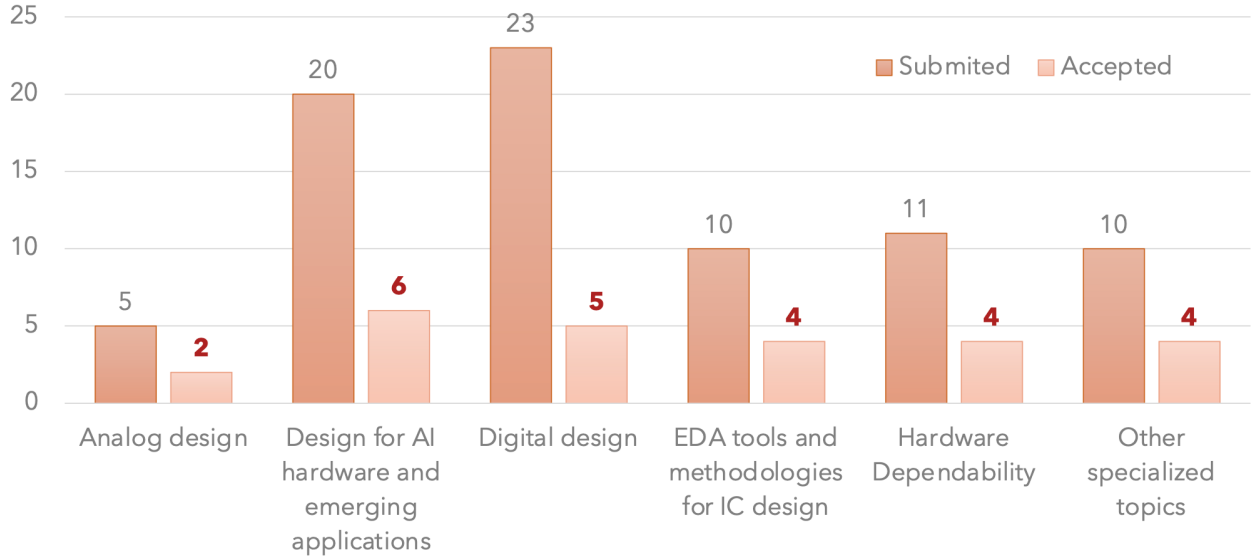
Said and Ioana provide details on VLSI-SOC 2024 that started today with 2 tutorials. Statistics follows:

- 102 valid submissions
  - 79 regular papers
  - 3 industrial contributions
  - 5 proposals for special sessions
  - 2 proposals for embedded tutorials
  - 13 PhD & Student Forum contributions

Topics of regular papers are distributed as follows:



Accepted papers per topics are as follows:



There will be three keynotes:

- Henk Corporaal (Technical University of Eindhoven): AI at the edge: Hype or Hope?
- Rajiv Joshi (IBM Research) Long Live Computing Technology
- Mark M. Tehranipoor (University of Florida): Secure Heterogeneous Integration and Advanced Packaging: New Attack Surfaces and Grand Challenges Ahead

The program is organized in 6 regular sessions, 4 special sessions, 2 embedded tutorials, 2 panel sessions, 1 industrial session, 2 poster sessions, and 1 PhD forum.

60 persons participated to the embedded tutorials.

Further details are reported in Annex I.

4. Status of VLSI-SOC 2025

Victor presented the status of VLSI-SOC 2025. It will be from October 12 to 15 in Puerto Varas (Chile).
The organizing committee is as follows:

General Chair	Pierre Emmanuel Gaillardon Victor Grimblatt	Utha Univesrity, USA Synopsys, Chile
Program Chair	Ricardo Reis Patrick Groeneveld	UFRGS, Brazil Cerebras, Stanford University, USA
Special Session Chair	Jorge Marin	AC3E, Chile
Local Organization Chair	Carlos Muñoz Local person	UFRO, Chile Universidad de los Lagos, Chile
Finance chair	Graziano Pravadelli	Universita di Verona, Italy
PhD and student Forum	Gonzalo Carvajal	USM, Chile
Publication chair	Carlos Silva	PUCP, Peru

Registration fees and expected attendees are:

Category	Early registration	Registration
IEEE	600	700
Non IEEE	800	900
IEEE Student	250	300
Student	300	350

Category	Estimated attendance
IEEE	85
Non IEEE	15
IEEE Student	20
Student	10

Further details are reported in Annex II.

5. Status of VLSI-SOC 2026

Florenc presented the status of VLSI-SOC 2026. It will be in Limassol (Cyprus) on October 5-7 or October 12-14.
General chairs will be Tiziana Margaria and Ian O'Connor, program chairs will be Panagiota Nikolaou, and Florenc Demrozi. The rest of the information are reported in annex III.

6. Any other business

Ricardo and Graziano reported info concerning sponsored conferences:

- SBCCI 24 had 300/400 participants in Joao Pessoa. In 2025 it will be in Manaus (Brazil)
- FDL 24 had 40 participants in Stockholm, Sweden . In 2025 it will be in Schloß Rheinfels, St. Goar, Germany

Membership to the WG was also discussed, particularly the issue of inactive members. To ensure active participation, the rules for membership need to be clarified. Members are expected to either attend WG meetings or participate in the TPC of VLSI-SOC or the conference itself at least once every two years. If a member remains inactive for two years, the WG chair will reach out via email to assess their interest and availability to continue as part of the WG.

Next meeting: at DATE 2025.

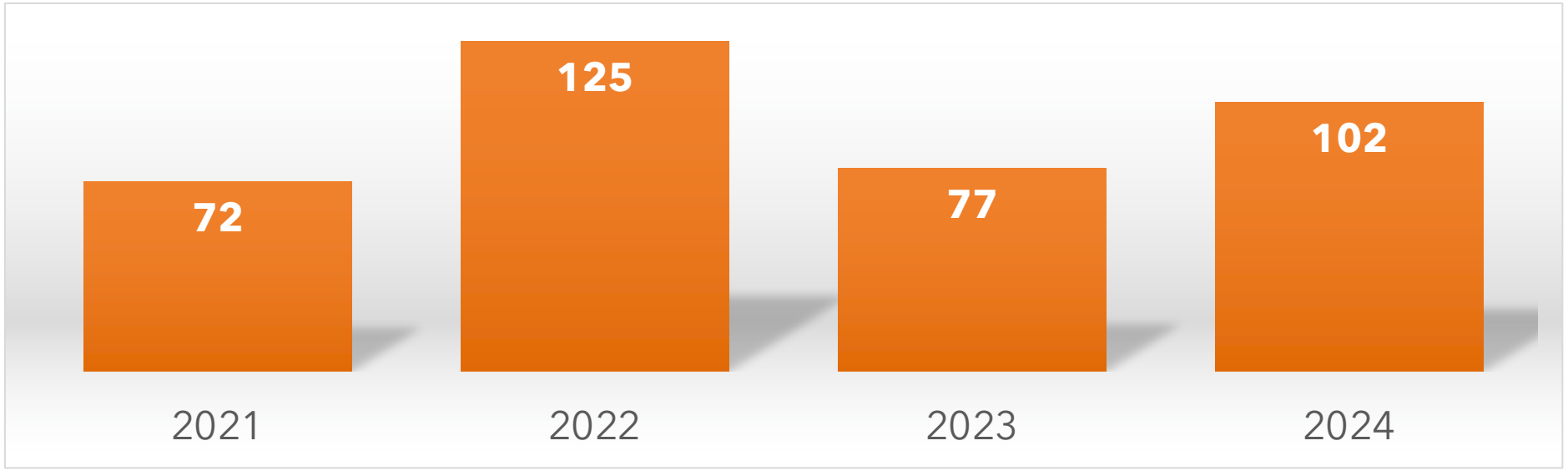
Annex I

Technical Program Overview

Ioana Vatajelu
VLSI-SoC 2024 Co-Program Chair

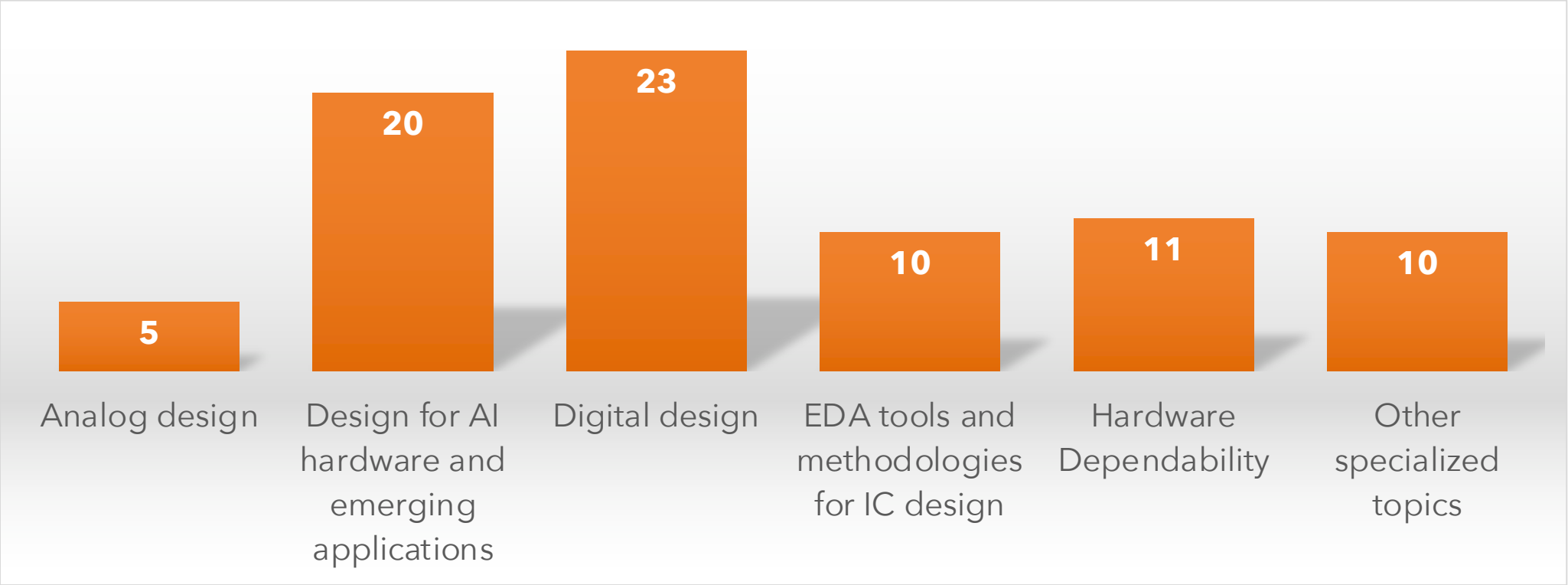
Submission Statistics

- Number of valid submissions: **102**
  - Regular Papers (novel and complete research work): **79**
  - Industrial Contributions: **3**
  - Proposals for Special Sessions: **5**
  - Proposals for Embedded Tutorials: **2**
  - PhD & Student Forum: **13**



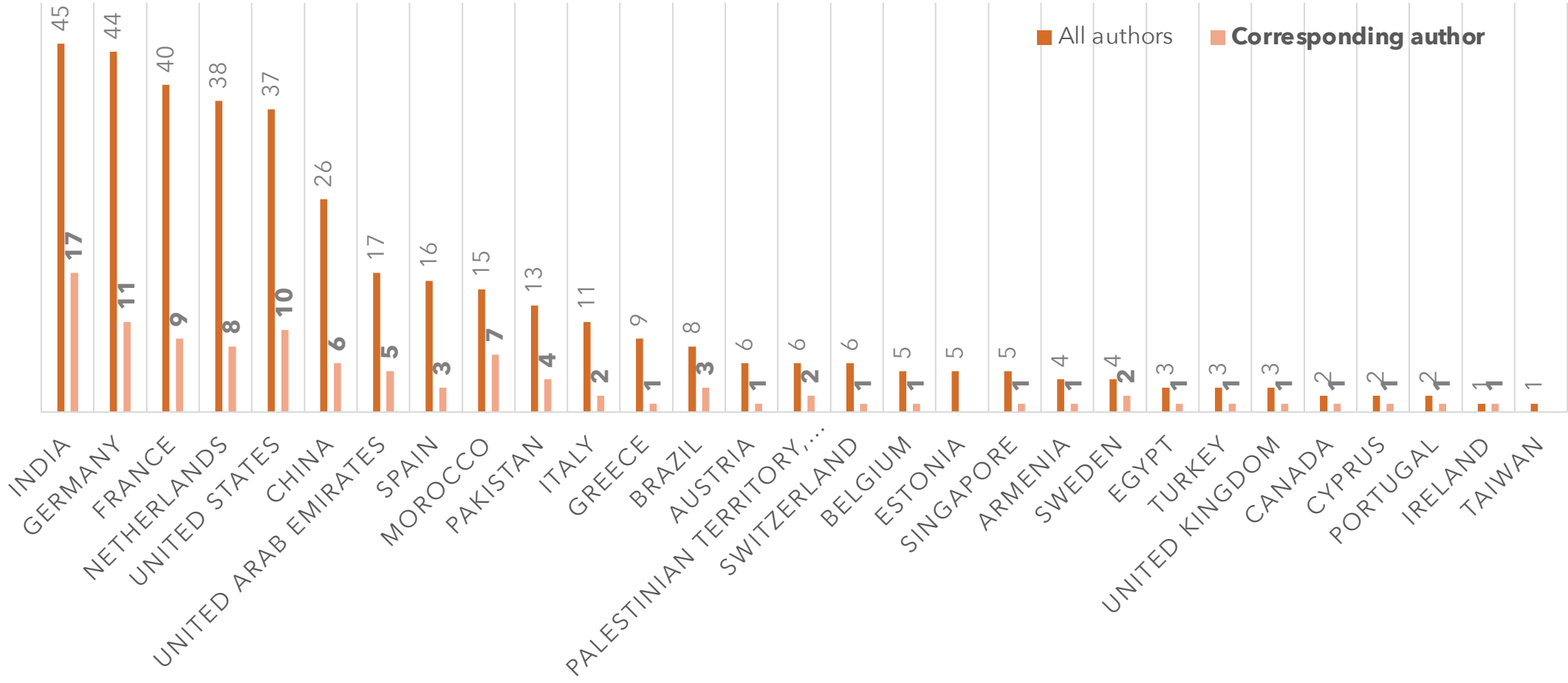
Submission Statistics

- Submissions per Topic



Submission Statistics

- Submissions per Country



Review Process

- Target reviews per paper: 4
- Involved reviewers: 83
- Overall reviews:
  - Assigned: 412
  - Reviewed: 367

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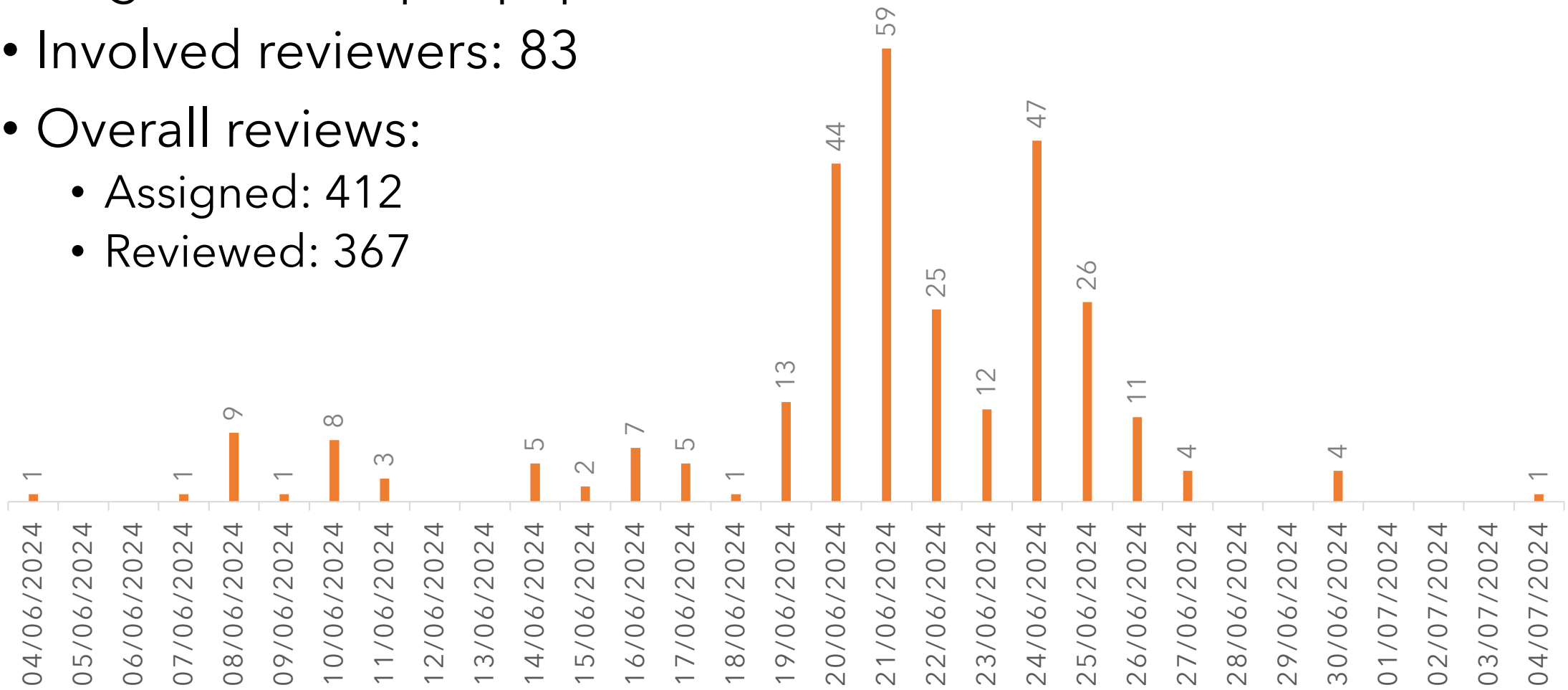

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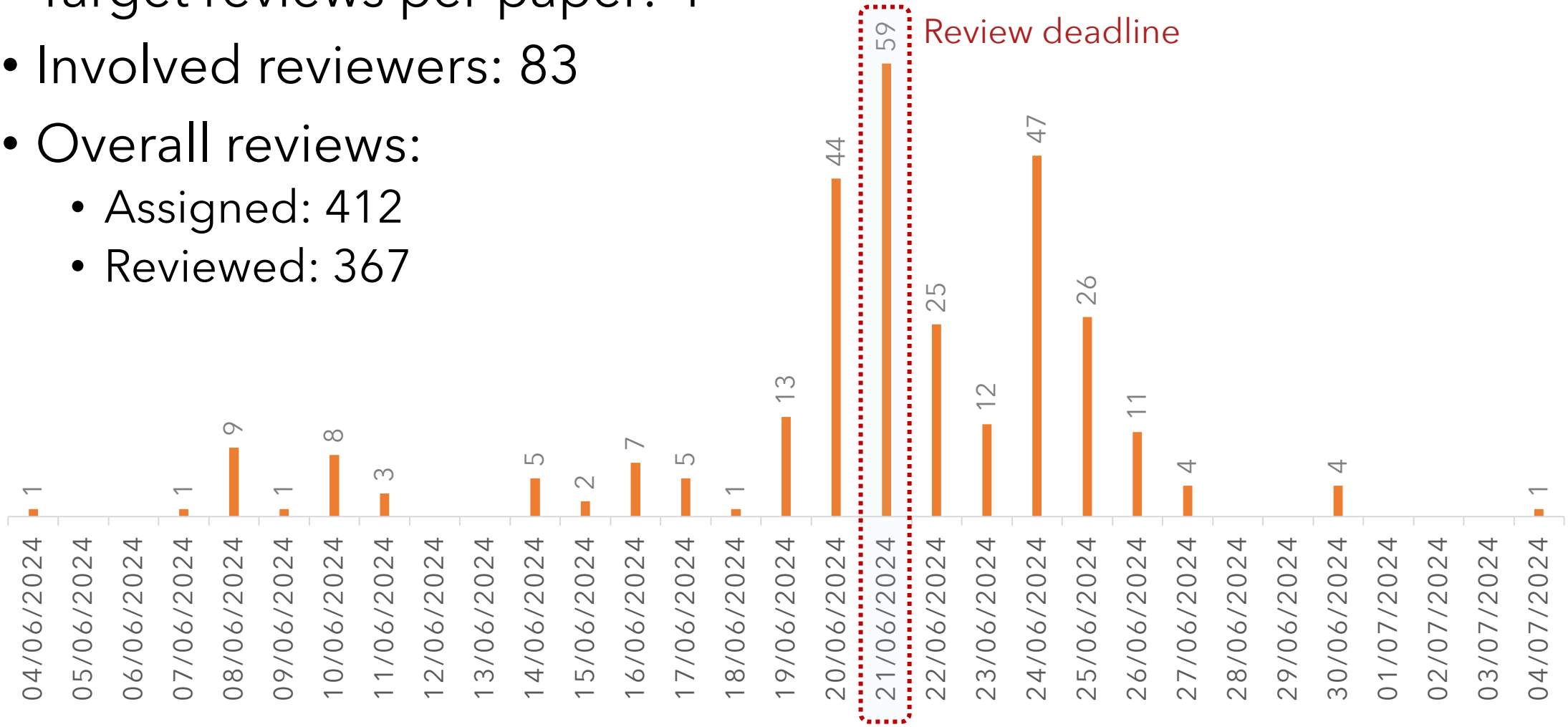
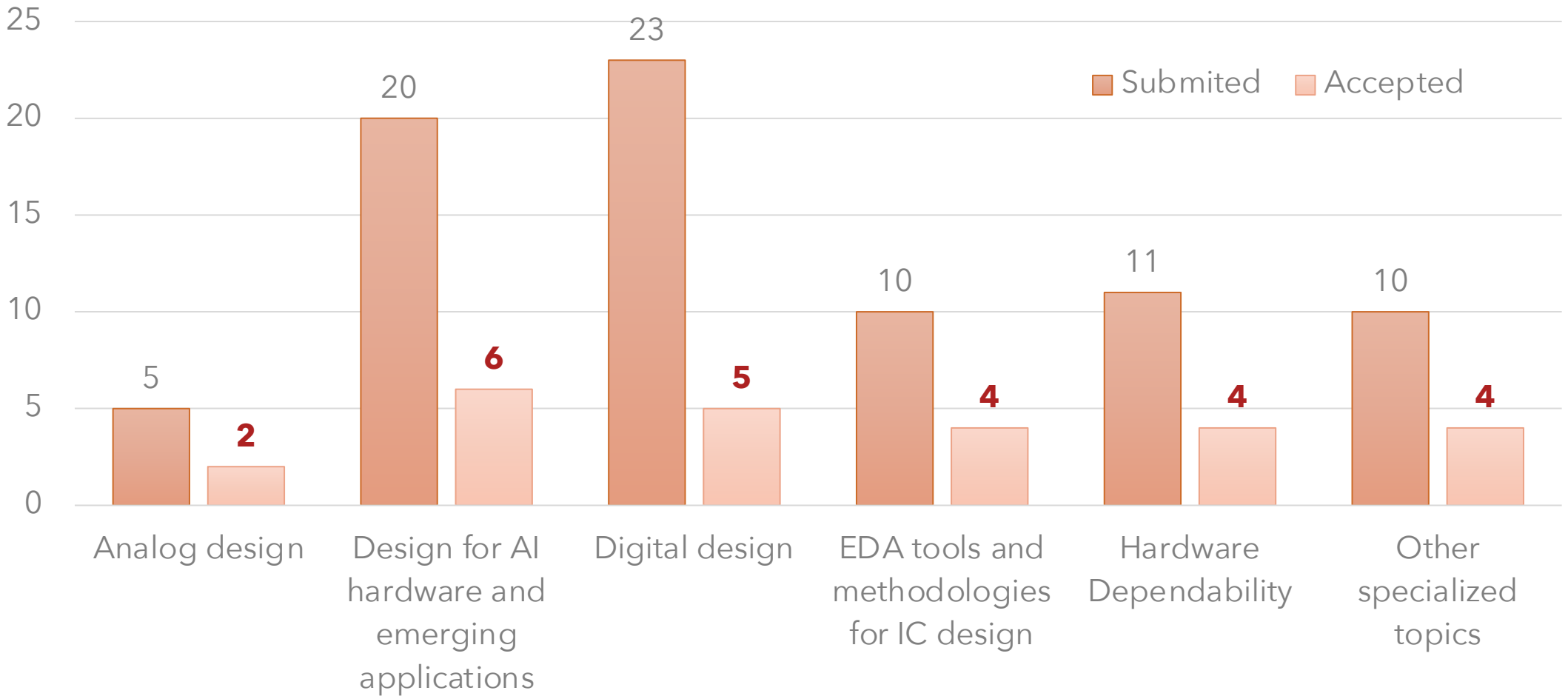


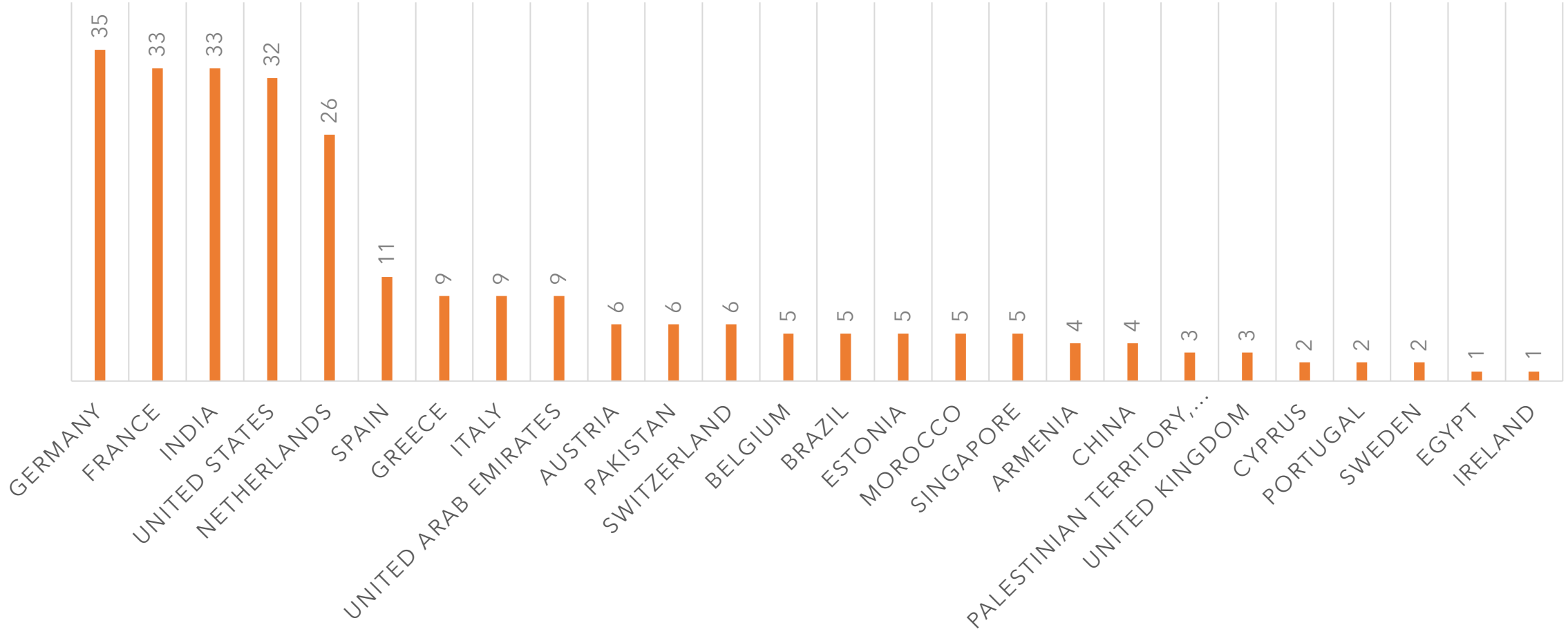
Review Process

- Target reviews per paper: 4
- Involved reviewers: 83
- Overall reviews:
  - Assigned: 412
  - Reviewed: 367
- **Accepted Papers**
  - **25 oral presentations (31% acceptance rate)**
  - **21 posters**

Accepted Papers per Topic



Accepted Papers per Country



Program Outline – Keynotes

In a few minutes: **Henk Corporaal** (Technical University of Eindhoven)

AI at the edge: Hype or Hope?

Tomorrow (09h00): **Rajiv Joshi** (IBM Research)

Long Live Computing Technology

Wednesday (09h00): **Mark M. Tehranipoor** (University of Florida)

Secure Heterogeneous Integration and Advanced Packaging:
New Attack Surfaces and Grand Challenges Ahead

Program Outline – Sessions

4 Special Sessions (Monday and Wednesday)

Reliability Assessment Of Neural Networks

IoT-Enabled Electronics For Smart Agriculture

Embedded Hardware Security: Primitives, Architectures, Test

Security By Design

2 Embedded Tutorials (Tuesday @ 14h00)

New Computing Paradigm For Large Language Models (LLMS)

Towards Silicon Lifecycle Management

Program Outline – Sessions

2 Panel Sessions

Today (18h00)

Semiconductor technology/ICT industry in MENA region: Hope or Hype?

Wednesday (16h00)

Challenges for Edge AI

Program Outline – Sessions

Today (14h00)

1 Industrial Session

Tuesday & Wednesday at 10h00

2 Poster Sessions

Monday 16h30

1 PhD Forum

Program Outline – Sessions

Today (14h00)

1 Industrial Session

Tuesday & Wednesday at 10h00

2 Poster Sessions

Monday 16h30

1 PhD Forum

Monday to Wednesday

6 Regular Sessions

4 Best Paper Award Candidates

Best Paper Award Candidates

Regular Session 1 – Security

Continuity in Security: Leveraging LLM for Translating Security Properties Across Hardware Designs

Bulbul Ahmed, Sujan Kumar Saha, Jingbo Zhou, Sohrab Aftabjahani, Mark Tehranipoor, Farimah Farahmandi

Regular Session 2 - Miscellaneous

Minimum Depth Quantum Modular Addition through Carry-Save Architecture

Siyi Wang, Eugene Lim, Xiufan Li, Jerrie Feng, Anupam Chattopadhyay

APPAMM: Memory Management for IPsec Application on Heterogeneous SoCs

Ayushi Agarwal, Radhika Dharwadkar, Isaar Ahmad, Krishna Kumar, P. J. Joseph, Sourav Roy, Prokash Ghosh, Preeti Ranjan Panda

Regular Session 4 – Design for AI

Adaptive block-scaled GeMMs on vector processors for DNN training at the edge

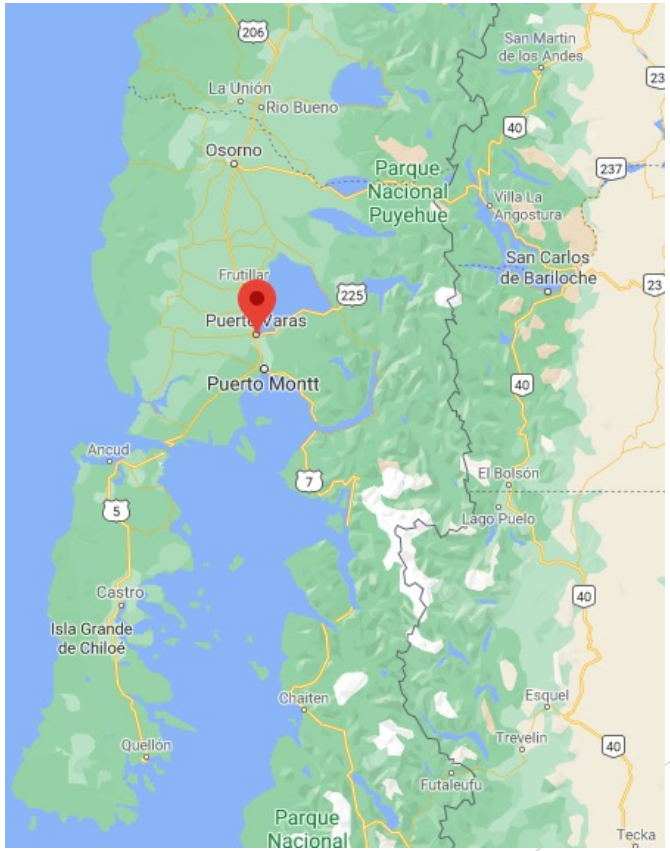
Nitish Satya Murthy, Nathan Laubeuf, Debjyoti Bhattacharjee, Francky Catthoor, Marian Verhelst

Annex II

VLSI SoC for a Sustainable World

October 12th - 15th, 2025

Puerto Varas, Chile

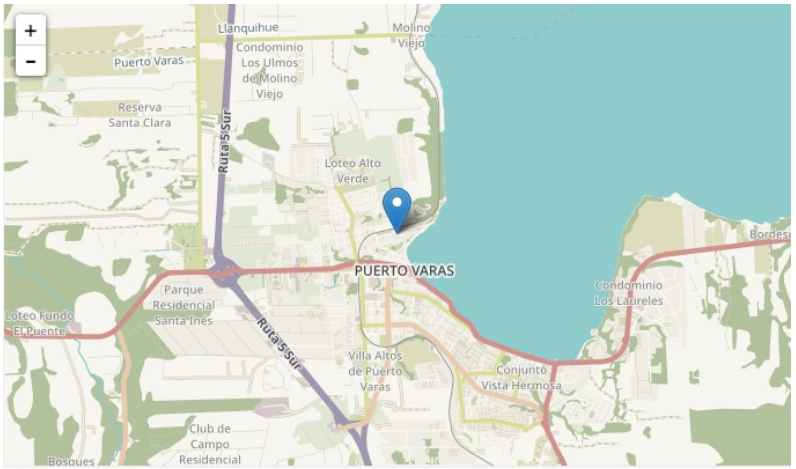


Puerto Varas

PUERTO VARAS EN 4K ULTRAHD (LAGOS / RÍOS / VOLCANES)

Venue

- Enjoy Puerto Varas (https://enjoy.loslagoshoteles.com/en/).
- 2 km from Puerto Varas downtown.
- 25 km from El Tepual airport (Puerto Montt).
- Several flights from Santiago every day.
- Several hotel accommodation such as swimming pool, beach on the lake Llanquihue, SPA Center, etc.).
- Close to other hotels and hostels in the city.
- 7 meeting rooms holding a total of 750 people.
- 84 guest rooms (price per room per night around US$ 150 – 180).
- Several tourist activities in Puerto Varas and around Puerto Varas.
- Local university in Puerto Varas, Universidad de los Lagos


Llanquihue
Molino Viejo
Condominio Los Ulmos del Molino Viejo
Puerto Varas
Reserva Santa Clara
Ruta 5 Sur
Loteo Alto Verde
PUERTO VARAS
Parque Residencial Santa Inés
Condominio Los Laureles
Loteo Fundo El Puente
Villa Altos de Puerto Varas
Conjunto Vista Hermosa
Club de Campo Residencial
Bosques

Organizing Committee

General Chair	Pierre Emmanuel Gaillardon Victor Grimblatt	Utha Univesrity, USA Synopsys, Chile
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Participants Fees and Attendance Estimation

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Category	Estimated attendance
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Budget (Estimation)

- Conference rooms: $ 15,000
- Coffee Breaks: $ 7,000 (2 per days, 3 days, 130 participants)
- Lunch: $ 14,000 (3 days, 130 participants)
- Social activities: $ 10,000 (Welcome reception and gala dinner – 130 participants)
- Keynote speakers: $ 10,000 (3 keynotes)
- Misc: $ 5,000
- Estimated total: $ 61,000 (prices could change based on inflation and other worldwide issues)
- Income: $ 81,000
  - Registration: $ 71,000
  - Sponsors: $ 10,000

Relevant Dates

- Abstract Submission; April 18
- Paper Submission: April 25
- Special session proposal: April 18
- Notification of acceptance: June 18
- Camera-ready: July 10


See you in Puerto Varas

Annex III

VLSI-SoC 2026

ESWEEK
2025 Sunday 28/9- Friday 03/10 (Defined)
2026 Sunday 27/9- Friday 02/10 (Very likely)

LIMASSOL

05 – 07 or 12 – 14
October 2026

UNIVERSITY OF LIMERICK
OLLSCOIL LUIMNIGH

University of Stavanger

International Accessibility

Cyprus provides a strategic geographic location connecting three continents, Europe, Asia, Africa with its excellent transportation and communications infrastructure.

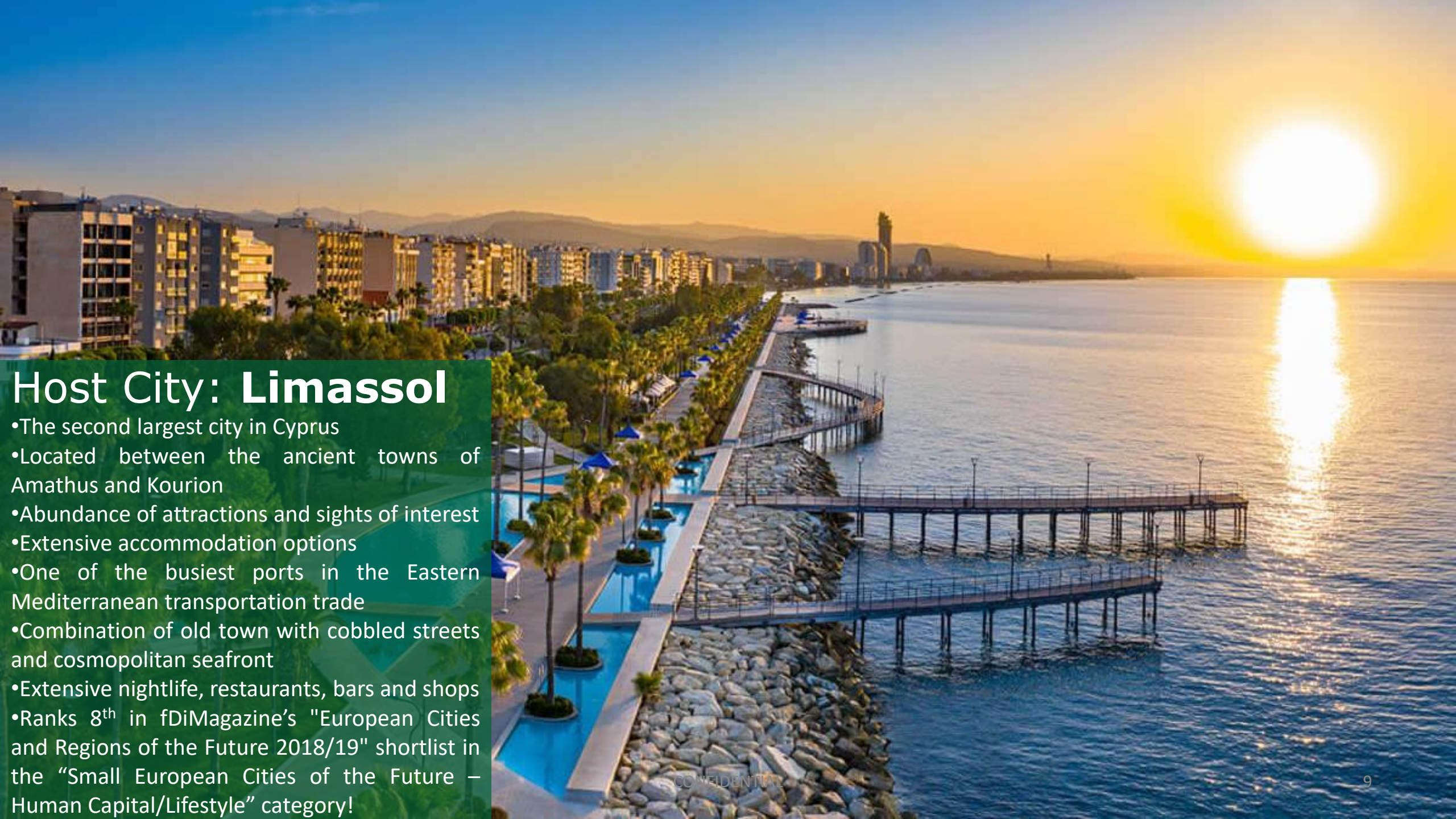
Visas

The Republic of Cyprus is a **full member of the European Union** from the 1stof May 2004, and the Eurozone from the 1st of January, 2008. As Cyprus is a candidate country bound to join the Schengen Area, residents of non-EU countries who hold valid multiple-entry Schengen visas must first pass through a full Schengen member territory in order to utilize the visa in Cyprus. Visas will be issued by all the Diplomatic Missions (Embassies and General Consulates) of the Republic of Cyprus, and by all the Honorary Consulates of the Republic of Cyprus abroad in their respective countries. Additionally, visas can also be issued by the British High Commissions / Embassies in many countries.

Airports

Larnaca International Airport (LCA) – the island's main airport, 35 minutes from venue hotel

Paphos International Airport (PFO) – 50 minutes from Limassol town



Host City: **Limassol**

- The second largest city in Cyprus
- Located between the ancient towns of Amathus and Kourion
- Abundance of attractions and sights of interest
- Extensive accommodation options
- One of the busiest ports in the Eastern Mediterranean transportation trade
- Combination of old town with cobbled streets and cosmopolitan seafront
- Extensive nightlife, restaurants, bars and shops
- Ranks 8th in fDiMagazine's "European Cities and Regions of the Future 2018/19" shortlist in the "Small European Cities of the Future – Human Capital/Lifestyle" category!

Venue
St. Raphael - 5*

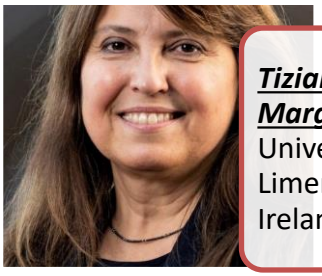
The St. Raphael Resort is located on one of the most renowned and largest beaches in Limassol, only a short coastal drive from the lively center of Limassol, approximately 15km away. There are shops, restaurants and bars within walking distance and a bus stop exactly outside the hotel. The hotel has 272 rooms and suites. Within the hotel there are 8 food and beverage outlets. A variety of conference rooms offer facilities and space to cater for any type of the event. The combination of space, service and facilities provided ensure St. Raphael Resort's place as one of the leading conference hotels in Limassol, Cyprus.

30 minutes from Larnaca Airport
50 minutes from Paphos Airport

Bus 30 stops right outside St. Raphael and connects the hotel with the whole coastline of Limassol

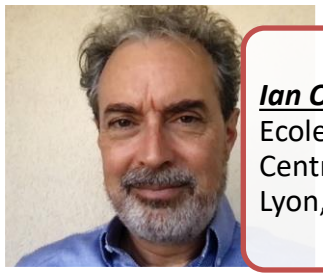
Preliminary Confirmed Committee Members

General Chair



Tiziana Margaria, University of Limerick, Ireland

General Chair



Ian O'Connor Ecole Centrale de Lyon, France

Program Chair

Panagiota Nikolaou University of Central Lancashire, Cyprus

Program Chair

Florenc Demrozi University of Stavanger, Norway

Publication Chair

Enrico Fraccaroli University of North Carolina at Chapel Hill, USA

Publication Chair

Industrial Chair

Industrial Chair

Tutorial Chair

Alberto Bosio Ecole Centrale de Lyon, France

Tutorial Chair

Special Session Chair

Pierluigi Nuzzo University of Southern California, USA

Special Session Chair

Theocharis Theocharides University of Cyprus, Cyprus

Finance Chair

Graziano Pravadelli University of Verona, Italy

Finance Chair

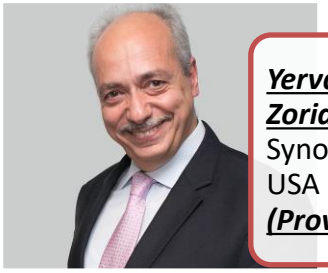
Preliminary Confirmed Committee Members

Publicity Chair

Daniele Jahier Pagliari
Politecnico of Turin, Italy

Publicity Chair

Award Chair



Yervant Zorian
Synopsys, USA
(Provisory)

Award Chair

Ph.D. Forum Chair

Michele Lora
University of Verona, Italy

Ph.D. Forum Chair

Panel Chair

Panel Chair

Web Chair

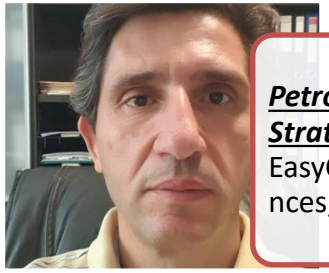
Matteo Iervasi
University of Stavanger, Norway

Web Chair

Local Arrangement

Nicolas Stratis
EasyConferences, Cyprus

Local Arrangement



Petros Stratis
EasyConferences, Cyprus

Local Arrangement

Contacted Keynote Speakers

Keynote 1*

Valeria Bertacco University of Michigan, USA

Keynote 2*

Giovanni De Micheli EPFL, Swizerland

Keynote 3*

Robert Wille TUM, Germany

Keynote 4*

Daniele De Venuto Politecnico of Bari, Italy

Keynote 5*

Expert form the Local University. Industry related

* Preliminary discussions


Looking forward to welcoming
VLSI-SoC 2026 in...
...Cyprus!