IFIP Working Group 10.5 Minute Meeting

March 25, 2024 17pm-18pm

Valencia (Spain) @DATE 2024

Notes taken by Graziano Pravadelli

Attendees in presence: Graziano Pravadelli, Chi Ying Tsui, Abe Elfadel, Ian O'Connor, Luis Miguel Silveira, Eugenio Villar, Matteo Sonza Reorda, Florenc Demrozi, Nicola Bombieri, Said Hamdioui, Joana Valajelu, Victor Grimblatta, Giovanni De Micheli, Tiziana Margaria, Jurgen Becker, Yuonquing Cheng.
Attendees in remote mode: Ricardo Reis, Katell Morin-Allory, Andrea Calimera, Fatigh Ugurdag, Ricardo Reis, Luc Claesen.

Apologies: Donatella Sciuto, Matthew Guthaus

Agenda

- Communications
- Mapping of competences
- Status of VLSI-SOC 2024
- Status of VLSI-SOC 2025
- Status of VLSI-SOC 2026
- Any other business

1. Communication

- The chair informs about the next conferences sponsored by the WG 10.5:
  - SBCCI 2024, João Pessoa, Paraíba, Brazil, September 2-6, Paper submission deadline: April 1
  - FDL 2024, Stockolm, Sweden September 4-6, Paper submission deadline: April 24
  - VLSI-SOC 2024, Tangier, Morocco, October 6-9, Paper submission deadline: May 3
- The chair remembers the deadline for nominating WG members for the IFIP awards and invites WG members to contact the award chair (Luis Miguel Silveira) in case they think someone deserves to be nominated.
  - IFIP Service Award: July 15
  - IFIP Silver Core Award: not possible this year, only on odd years
  - IFIP Fellow Award: April 30

2. Mapping of WG competences

A final set of 12 topics and 38 subtopics have been selected starting from a matrix composed of 46 topics and 40 application fields.
The selected topics are:

- AI architectures and applications
- Analog, digital and mixed-signal circuits design and syntesis
- Communication architectures and technologies
- Computing paradigms
- Embedded system design
- Emerging technologies and applications
- Smart systems, devices and applications
- Low-power, energy-efficient and thermal-aware design
- Security
- Sensors and signal processing
- System specification, simulation and verification
- Test and dependability

Per each topics, two topics leaders have been defined. They are in charge of:

- Describing the topic by including keywords (core technologies)
- Mapping members on the topics
- Creating the core technology cloud

The distribution of the topics leaders is as follows:

Leaders	Topics	Subtopics					
Claesen, Silveira	AI architectures and applications	App. of AI and ML	Arch. for AI and ML				
Ugurdag, Reis	Analog, digital and mixed-signal circuits design and syntesis	Digital circuits	Analog devices	High-level and logic-level synthesis	Reconfigurable architectures and systems	Mixed signal	SoC
Becker, Soudris	Communication architectures and technologies	5G/6G technologies	RF	Network on Chip			
O'Connor, Vatajelu	Computing paradigms	Quantum computing	Approximate computing	Evolutionary computing	In-memory computing		
Bombieri, Villar	Embedded system design	Embedded software and toolchains	Edge computing	Cloud computing	Parallel computing and architectures		
Hamdioui, Guthaus	Emerging technologies and applications	Emerging technologies					
Mohanty, Grimblatt	Smart systems, devices and applications	IoT, industrial IoT, IoMT	Smart systems	Cyber-physical systems	Big data		
Calimera, Gaillardon	Low-power, energy-efficient and thermal-aware design	Cryogenic processors	Low-power design				
Katkoori, Elfadel	Security	Hardware security					
Tsui, Demrozi	Sensors and signal processing	Sensors and biosensors	Signal processing				
Morin-Allory, Margaria	System specification, simulation and verification	Simulation	Verification	System specification and modelling	Hardware description languages	Prototyping and virtual prototyping	
Sonza Reorda, Mir	Test and dependability	Design for testability	Fault tolerance	Fault modelling	Testing	Reliability	

EDA tools

Currently, 7 out of 12 topic leaders have sent the topic descriptions. The chair kindly asks to complete the missing descriptions in the coming days.
The next steps are then:

- looking for overlapping and solving in case;
- provide feedback on the descriptions;
- indicate members interested in the topics;
- identifying underrepresented topics and inviting new members.

3. Status of VLSI-SOC 2024

Said presents the status of VLSI-SOC 2024 in Tangier, Morocco. He informs that the organizing committee is almost set up, but some co-chair roles are still missing. He kindly invites WG members to propose themselves to close the following holes:

- Tutorial co-chair
- Industrial session co-chair
- PhD forum co-chair
- Sponsoring co-chair

The web site is online and molesystem will be used as the submission system.
Deadline for paper submission is May 3, for special session is May 20, for PhD and student forum is May 10.
The CFP has been updated as required by the steering committee. Printed copies are distributed during DATE 2024.
The program includes, in addition to the traditional format, 2 full-day tutorials on Saturday 5 and Sunday 6 of October about, respectively, AI: from fundamentals to applications, and Computers: from Intel 4004 to Neuro Chips.
Two keynotes have been already identified:

- Rajiv Joshi, IBM Research, "Long Live Computing Technology"
- Henk Corporaal, Technical University of Eindhoven, "AI at the edge: Hype or Hope?"

The third keynote speaker could be Mark M. Tehranipoor (University of Florida) to talk about security.
A fourth keynote by a woman would be appreciated.
The social activities include visiting the Hercules cave, the point where the Mediterranean meets the Atlantic Ocean, the old city with the famous Cafè Hafa, etc.
The list of TPC members will be available in the web site in two weeks.

4. Status of VLSI-SOC 2025

Victor presents the status of VLSI-SOC 2025 in Puerto Varas, Chile. The conference location will be Enjoy Puerto Varas (https://enjoy.loslagoshoteles.com/en/). It has 84 guest rooms (price per room per night around US$ 150 – 180), but many other (cheaper) hotels are located near the conference venue.
The organizing committee is under definition. Key roles are:

- General chairs: Victor Grimblatt, Pierre Emmanuel Gaillardon
- Program chairs: Ricardo Reis, Patrick Groeneveld
- Special session chair: Jorge Marin
- Local organizing chair: Carlos Muñoz
- Publication chair: Carlos Silva

WG members that are interested in cooperating to the organization can contact Victor.
Estimation of the budget and registration fees have are reporte as follow:

Participants Fees and Attendance Estimation

Category	Early registration	Registration
IEEE	600	700
Non IEEE	800	900
IEEE Student	250	300
Student	300	350

Category	Estimated attendance
IEEE	85
Non IEEE	15
IEEE Student	20
Student	10

Budget (Estimation)

- Conference rooms: $ 15,000
- Coffee Breaks: $ 7,000 (2 per days, 3 days, 130 participants)
- Lunch: $ 14,000 (3 days, 130 participants)
- Social activities: $ 10,000 (Welcome reception and gala dinner - 130 participants)
- Keynote speakers: $ 10,000 (3 keynotes)
- Misc: $ 5,000
- Estimated total: $ 61,000 (prices could change based on inflation and other worldwide issues)
- Income: $ 81,000
  - Registration: $ 71,000
  - Sponsors: $ 10,000

5. Status of VLSI-SOC 2026

Tiziana presents the status of VLSI-SOC 2026 in Limassol, Cyprus. The conference dates will be decided between Oct 5-7 and Oct 14-16, depending on the ESWEEK dates that will be announced in the coming 3 months.
The venue will be at the St. Rapahel 5* hotel, 30 minutes from the Larnaca airport.
Registration fees and accommodation cost will be in line with the past editions.
The organizing committee is under definition. Persons that are available to take key roles, at the moment, in addition to Tiziana Margaria and Florenc Demrozi are: Maria Michale (University of Cyprus), Theocharis Theocharides (University of Cyprus), Yervant Zorian (Synopsys) Enrico Fraccaroli (UNIVR), Ian O'Connor (Ecole Centrale de Lyon), Alberto Bosio (Ecole Centrale de Lyon), Pierluigi Nuzzo (University of Southern California), and Daniele Jahier Pagliari (Politecnico di Torino.
WG members that are interested in cooperating to the organization can contact Tiziana Margaria.

6. Any other business

None

Next meeting: at DAC 2024.