IFIP Working Group 10.5 Minute Meeting

October 02, 2022 5pm-7:30pm

Patras (GR)

Notes taken by Graziano Pravadelli

Attendees in presence: Ibrahim Elfadel, Victor Grimblatt, Said Hamdioui, Odysseas Koufopavlou, Salvador Mir, Graziano Pravadelli, Fatih Ugurdag.
Attendees in remote mode: Andrea Calimera, Tiziana Margaria, Katell Morin-Allory.

Apologies: Nicola Bombieri, Luc Claesen, Giovanni De Micheli, Matthew Guthaus, Srinivas Katkoori, Ricardo Reis, Luis Miguel Silveira, Matteo Sonza Reorda, Chi Ying Tsui.

Invited: Lutfi Albasha (program co-chair of VLSI-SOC 2023)

Agenda

1. Communications
2. Status of VLSI-SOC 2022
3. Status of VLSI-SOC 2023
4. Ideas for VLSI-SOC 2024
5. Mapping of WG competences
6. Any other business

1. Communication

- WG 10.5 web site has been restyled. It is now optimized also for mobile devices. A page has been added for videos. It will also contain the mapping of WG 10.5 competences in the near future
- F. Anceau workshop was held in Grenoble on June 14 with more than 50 participants. Videos of the workshop are now in the WG 10.5 web site.
- IFIP awards 2022
    - 4 nominees for the IFIP service award. Informal news from the TC 10 chair is that all has been awarded
    - Start thinking about award candidates for 2023 (IFIP fellows, IFIP silver core award, IFIP service award and WG 10.5 meritorious service award). Propose candidates to the award chair (L. M. Silveira)
- VLSI-SOC 2021 book is available online: https://link.springer.com/book/10.1007/978-3-031-16818-5
- 2022 IFIP report has been sent last July to the TC 10 chair and it is available on the WG 10.5 web site

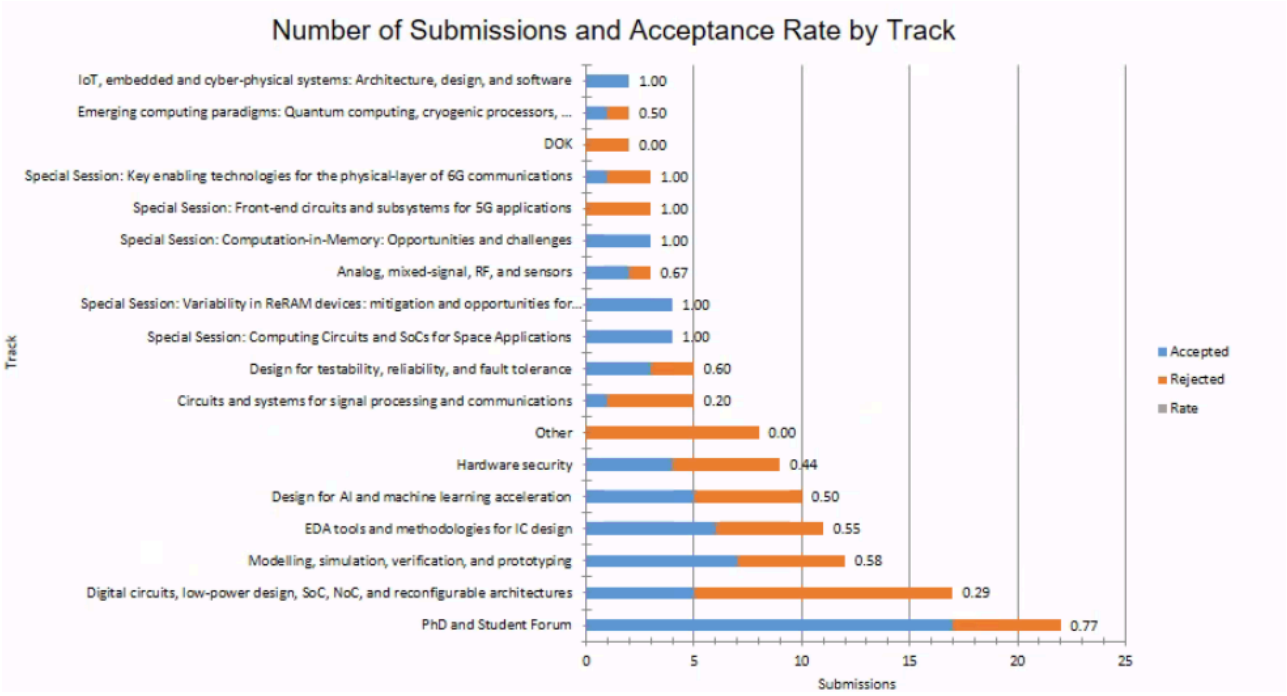
2. Status of VLSI-SOC 2022

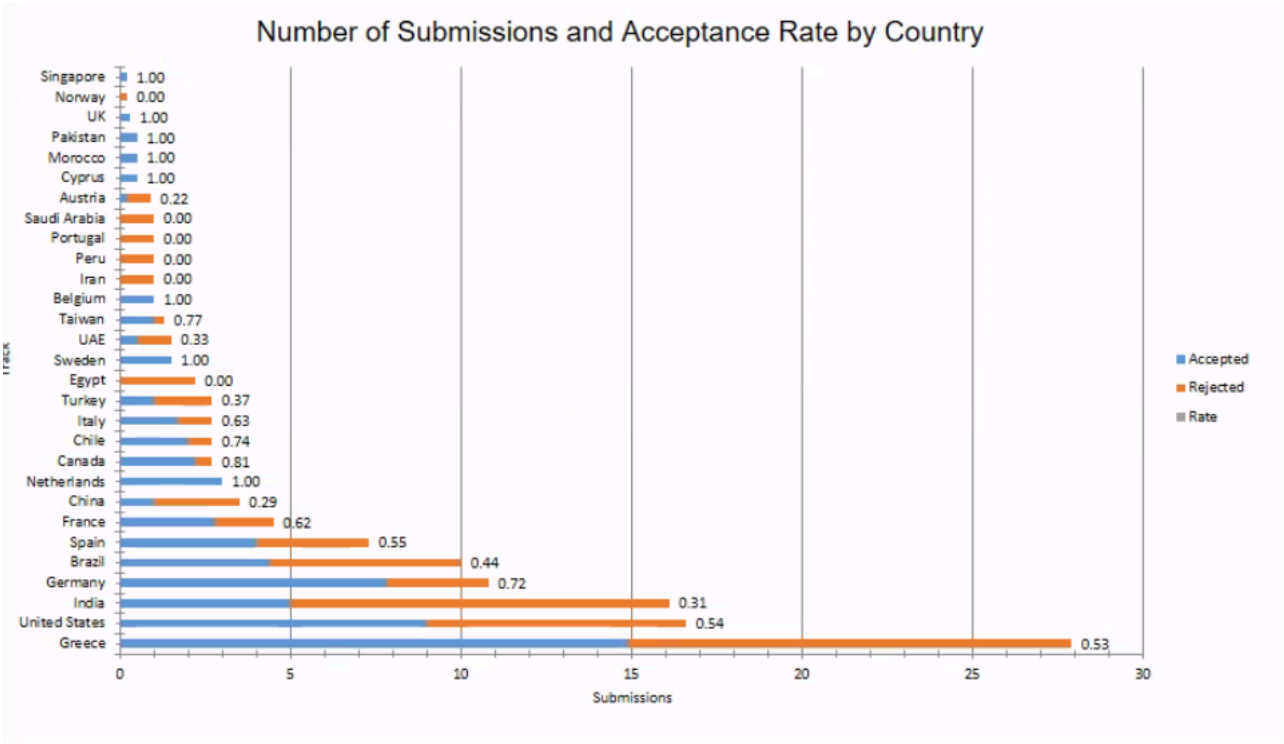
Odysseas Koufopavlou (General chair) and Vassilis Paliouras (program chair) presented the status of VLSI-SOC 22 during the TPC meeting that preceded the WG 10.5 meeting. Main information follows:

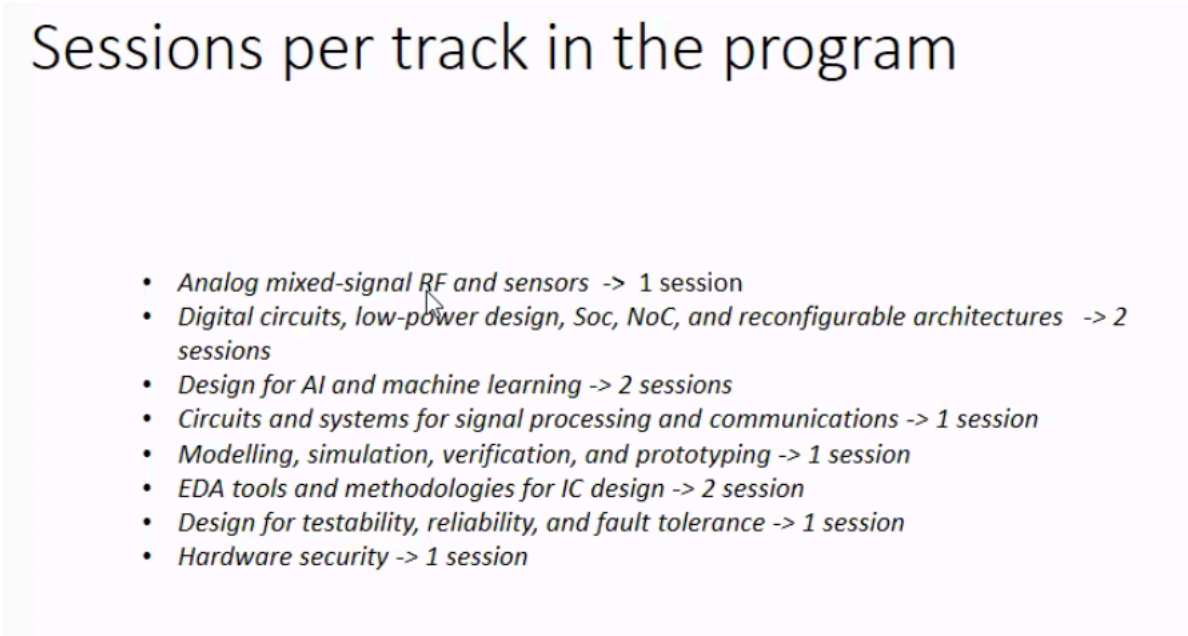
- The conference will run in presence in the period October 3-5. 10 papers will be presented online
- 10 tracks have been defined:

track	submissions
Analog, mixed-signal, RF, and sensors	3
Circuits and systems for signal processing and communications	5
Design for AI and machine learning acceleration	10
Design for testability, reliability, and fault tolerance	5
Digital circuits, low-power design, SoC, NoC, and reconfigurable architectures	17
EDA tools and methodologies for IC design	11
Emerging computing paradigms: Quantum computing, cryogenic processors, ...	2
Hardware security	9
IoT, embedded and cyber-physical systems: Architecture, design, and software	2
Modelling, simulation, verification, and prototyping	12
Other	10
PhD and Student Forum	22

- Number of total submissions: 125, including PhD and students forums and special sessions (in average 3/4 reviews per paper)
- Accepted contributions:
  - Main conference: 56 (43 for oral presentation in 11 sessions + 13 posters)
  - Special session: 16 papers (5 sessions)
  - PhD Forum: 10
  - Student Forum: 7
- 19 papers will be invited to submit an extended version for the Springer book







- The program includes also 3 keynotes:
  - Prof. Levantino (Politecnico di Milano, Italy): "***Designing Phase-Locked Loops in Modern CMOS Technologies***"
  - Prof. Drechsler (University of Bremen, Germany): "***Preserving Design Hierarchy Information for Polynomial Formal Verification***"
  - Prof. Çetin Kaya Koç (University of California Santa Barbara, USA): "***Challenges in Hardware Implementations of Fully Homomorphic Encryption Algorithms***"

4. Status of VLSI-SOC 2023

Lutfi Albasha (program co-chair) summarised the status of VLSI-SOC 2023 in Dubai (UAE).

- Dates: October 16-18 2023

- Location: Dubai Festival City
- Negotiation is ongoing for the conference venue (alternatives: Convention Centre or Holiday Inn Ballrooms)
- Theme of the conference: VLSI SoC Innovations for Trustworthy AI
- Opening ceremony and one keynote will be at American University of Sharjah (dedicated buses will be arranged for all participants)
- Current sponsors: IFIP, IEEE CEDA, IEEE CAS, American University of Sharjah, Khalifa University, Rodhe&Swarz, Cadence, Keysight, University of Sharjah
- Organizing committee: completed.

General co-chairs:	Fadi Aloul (American University of Sharjah, UAE) Luis Miguel Silveira (Technical University of Lisbon, Portugal)
Program co-chairs:	Lutfi Albasha (American University of Sharjah, UAE) Abe Elfadel (Khalifa University, UAE)
Special session co chairs:	Usman Tariq (American University of Sharjah, UAE) Said Hamdioui (Delft University of Technology, The Netherlands) Hasan Nashash (American University of Sharjah, UAE)
General Relations Chair	Assim Sagahyroon (American University of Sharjah, UAE)
Social Program Chair	Abdulrahman Al-Ali (American University of Sharjah, UAE)
Ph.D. forum chair:	Mahmoud H. Ismail (American University of Sharjah, UAE)
Students forum chair:	Amer Zakaria (American University of Sharjah, UAE)
Industrial chair:	Fabrizio De Paolis (European Space Agency, UK)
Local chair:	Nasser Qaddoumi (American University of Sharjah, UAE)
Publication chair:	Hasan Mir (American University of Sharjah, UAE) Ricardo Reis (UFRGS, at Porto Alegre, Brazil) Salvador Mir (TIMA Laboratory, France)
Publicity co-chairs:	Sohaib Majzoub (University of Sharjah, UAE) Soliman Mahmoud (University of Sharjah, UAE) Fatih Ugurdag (Ozyegin University, Turkey) Matthew Guthaus (UC Santa Cruz, USA) Graziano Pravadelli ((University of Verona, Italy)
Registration Chair:	Mohamed Hassan (American University of Sharjah, UAE)
Administration:	Shena Rosa (American University of Sharjah, UAE)

- Preliminary CFPs for conference, PhD Forum and Student Forum are ready
- Proposed technical tracks

Topics of interest include (but not limited to):

1. Analog, mixed-signal, RF, and sensors
2. Digital circuits, low-power design, SoC, NoC, and reconfigurable architectures
3. Design for AI acceleration and machine learning for SoC design
4. Signal processing and communications for 6G
5. Modelling, simulation, verification, and Prototyping
6. EDA tools and methodologies for IC design
7. Design for testability, reliability, and fault tolerance
8. Research in UAE: Biomedical, Space and Hardware security
9. IoT and CPS for Smart Cities and Transportation
10. Emerging computing paradigms: Quantum computing, cryogenic processors

- Web site is ready at https://www.vlsisoc2023.com
  - To be redirected to www.vlsi-soc.com by asking to Matthew Guthaus
- Application submitted to IEEE

A discussion followed:

- Victor proposed to promote the participation of people from industries. This requires something more than appointing an industrial chair. Victor remembered participation of industry to conferences is extremely win-win for both academia and industry.
    - Proposals discussed in the meeting that can be implemented starting from VLSI-SOC 2023 were:
        - Adding a track dedicated to industrial papers/case studies. This is not intended as a special session. It is a regular track, whose reviewers should not just look at innovation, but also to other aspects relevant for industries (e.g., case studies, performance improvements, EDA tool experiences, etc.). The submission of a 6-page papers would be not necessary as authors from industries generally do not have time for preparing the paper.
        - Extending the organizing committee with some persons from industries in key roles.
        - Having lunch keynotes from industry.
- Graziano remembered a multiyear MOU must be submitted to IEEE. As the application has been already submitted, Lutfi should contact IEEE specifying we are interested in a 3-year MOU
    - https://ieeemce.org/planning-basics/ieee-conference-application-business-essentials/mou-approval/#!/workspaces/
- Graziano remembered to submit the application to IFIP as well at the following link:
    - https://www.ifip.org/events/
- Several members proposed to start having an online TPC meeting for VLSI-SOC, from 2023 in advance, at the end of the review process for discussing the papers to be accepted/rejected.
    - A half-day TPC meeting with separate rooms for every track will guarantee to discuss border line papers and avoid cases where very good technical papers risk to be rejected or well-written papers, but without novelties, risk to be accepted due to the low confidence of reviewers, when the acceptance/rejection is made just by comparing the scoring without live discussions of the reviewer comments.
    - Graziano will update the VLSI-SOC conference guidelines accordingly.

5. Status of VLSI-SOC 2024

Said Hamdioui summarizes key points for the organization of VLSI-SOC 2024 in Tangier.

- A structure of the overall program was presented, including 2 tutorials on Sunday before the conference, 3 keynotes, 2 panels, regular and special sessions, poster session, and PhD/student forums.
- He proposed to identify and involve women for some of the key roles and to create a TPC with a mix of junior and senior members to guarantee the evolution of the conference in the future years.
- He proposed to discuss a long-term vision of VLSI-SOC inside the steering committee.

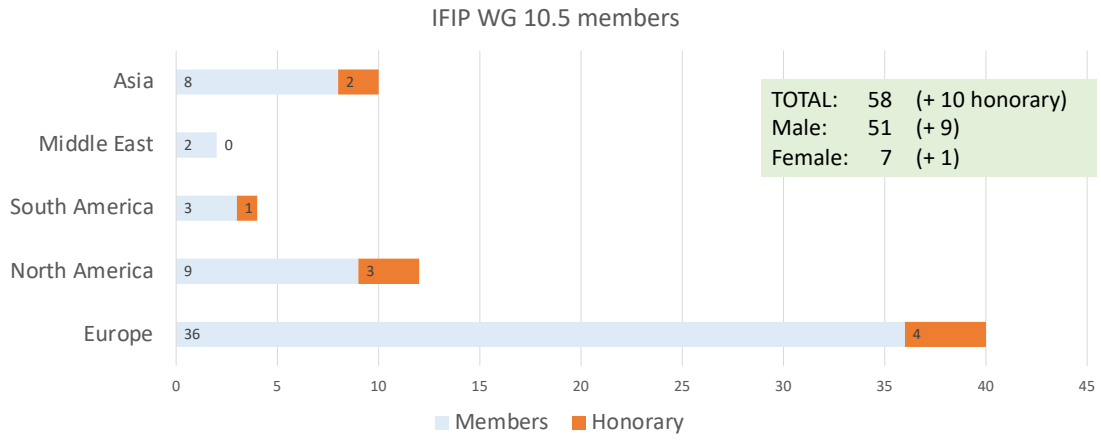
7. Mapping of WG competences

Graziano remembers the idea of the mapping. The process has started last May with a survey sent to all WG 10.5 members asking for topics of interest and related application domains and core technologies. From the analysis of the results the following main aspects appear:

- Actual composition of the WG is as follows. 24 members out of 58 filled in the survey

IFIP WORKING GROUP 10.5
Design and Engineering of Electronic Systems

Actual composition of the WG 10.5



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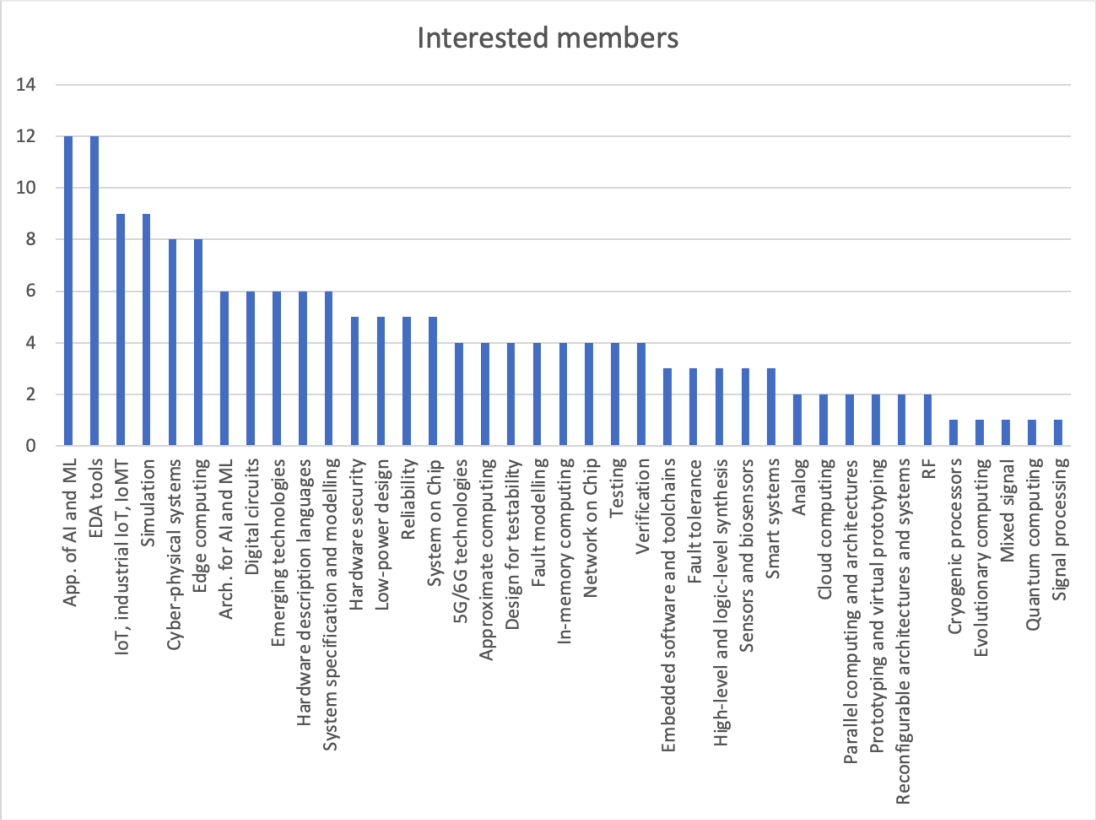
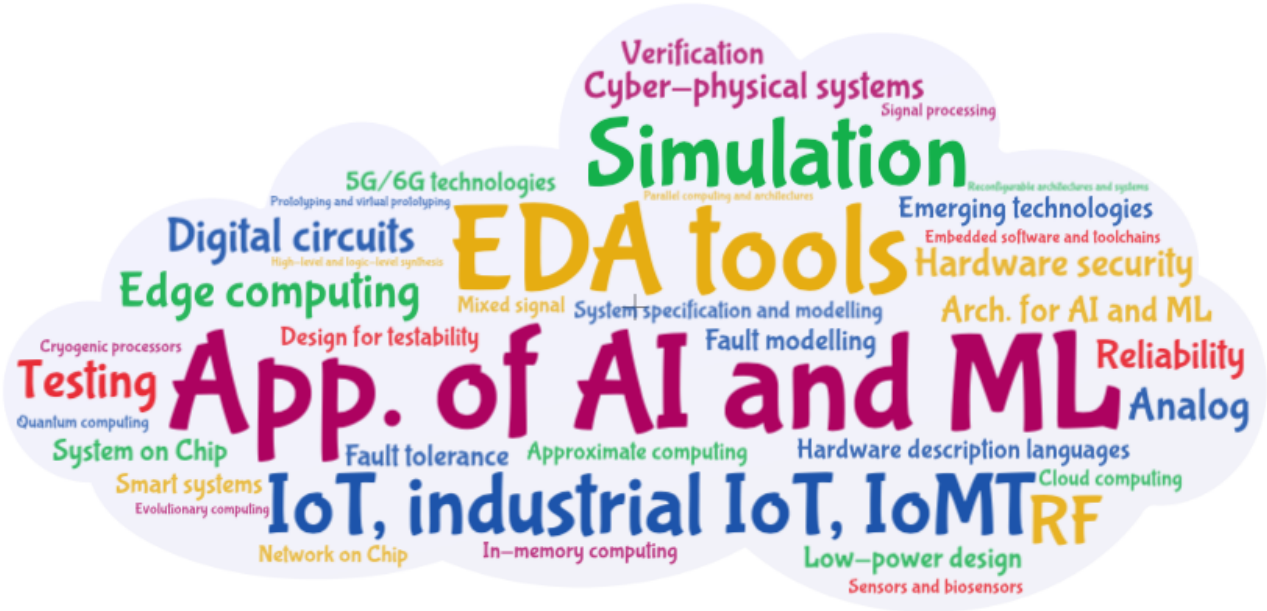
- 39 topics have been identified. Interested members are distributed as follows:



- A words cloud view of the more interesting topics for WG 10.5 members appears as follows:



- 54 application domains were associated to the topics. The corresponding words cloud is as follows:

- Overall, from topics and application domains, a 54 x 39 matrix derived.
- Finally, concerning the core technologies (more than 130) associated by the members to their topics of interest, the analysis of the result was difficult because there is not a homogeneous view of what a core technology is. In some cases, the respondents indicated an application field, in other cases they wrote a subtopic, in others a method, etc.. The overall words cloud appear as follows:

- **Further steps will be:**
  - To send the matrix to the WG members for the final collection of information. Each member will be required to put "x" on the cells representing the matching of his/her interests with the application domains where he/she works.
  - To identify a responsible for each topic with the role of briefly describing the topic according to the related application domains and core technologies
  - To collect a more homogeneous view of the core technologies.
  - To add a new page in the WG web site with the description of topics and the list of interested members, and the words cloud of the related core technologies.

8. Any other business

None

Next meeting: to be defined (maybe at DATE in April 2023).