IFIP Working Group 10.5 Minutes Meeting

March 02, 2021

Virtual meeting

Notes taken by Graziano Pravadelli

Attendees: Graziano Pravadelli, Victor Grimblatt, Ricardo Reis, Fatih Ugurdag, Luc Claesen, Maciej Ogorzalek, Chi Ying Tsui, Nicola Bombieri, Tiziana Margaria, , Ahmed Jerraya, Dominique Borrione, Salvador Mir , Srinivas Katkoori, Ian O'Connor, Eugenio Villar, Luis Miguel Silveira, Odysseas Koufopavlou, Sara Vinco, Yuanquing Cheng, Katell Morin-Allory, Achim Rettberg

Apologies: Donatella Sciuto, Nikil Dutt, Alexander Stempkovsky

Invited: Anupam Chattopadhyay, Seokhyeong Kang

Agenda

1. Communications
2. New member candidatures: prof. Seokhyeong Kang
3. Status of VLSI-SOC 2021
4. Status of VLSI-SOC 2022
5. Ideas for VLSI-SOC 2023
6. Francois Anceau workshops
7. Mapping of WG competences
8. Any other business

1. Communication

Prof. Achim Rettberg (TC 10 chair) reports the following information:

- We have a drop in income due to the corona time, but the big issues was the portfolio from IFIP. We are still move to a different bank. TC 10 is anyway quite good.
- There will be a new IFIP President. There are two candidate. The voting will be in the next general assembly.

Graziano reports the following information:

- There is the possibility of publishing best paper of IFIP conferences on the IFIP Select journal. Ricardo asks if this is intended to republish the same paper of the conferences without extension. Achim answers that in the past no extension was necessary, but

now the paper must be extended. Ricardo remembers that for VLSI-SOC the extended versions of best papers are published in the Springer Book. Graziano asks Achim to investigate during the general assembly about the possibility of moving the extended version of VLSI-SOC best papers towards a (Springer?) journal by preserving the royalties mechanism of the current book. This will better for authors as journal papers are generally best evaluated than book chapters.

- The 2020-2021 annual report of the WG activities has been sent to Achim last July.
- Springer Book concerning VLSI-SOC 2020 has been published
- IFIP nominations for both Silver Core and IFIP fellow have been submitted in time. No news at the moment
- A special session has been organized by Sara about «Design and Engineering of Electronic Systems» with three contributions from Eugenio, Tiziana and Victor
- In occasion of the IFIP60 Jubilee two webtalks have been proposed by WG 10.5 Both has been accepted:
    - Sept. 13 2021 @2pm CEST: **Digital Twin for Cyber Physical Production Systems**
        - Panelists: Franco Fummi (Univ. of Verona, Italy), Arquimedes Canedo (Siemens, USA), Samarjit Chackraborty (UNC. at Chapel Hill, USA)
        - Moderators: Achime Rettberg (Univ. of Applied Science Hamm-Lippstadt, Germany), Graziano Pravadelli (Univ. of Verona, Italy)
    - Oct. 25 2021 @5pm CEST: **Trends on Computing Systems**
        - Panelists: Nikil Dutt (Univ. of California Irvine, USA), Donatella Sciuto (Politecnico di Milano, Italy), David Atienza (EPFL, Switzerland), Victor Grimblatt (Synopsys, Chile)
    - Moderators: Graziano Pravadelli (Univ. of Verona, Italy)
- Many other initiatives related to the IFIP60 Jubilee are available at https://ifip.org/jubilee60/?r=about

2. New member candidatures

We have 1 new candidature by Prof. Seokyeong Kang from POSTECH, Korea (preliminary approved on July 2021 by electronic voting).
The candidate presents his research activities which focus in particular on design automation, deep learning accelerators and multi-valued logic.
After the presentations, we unanimously approved the admission of the candidate to the working group.

3. Status of VLSI-SOC 2021

Anupam and Victor present the status of VLSI-SOC 21.

- The conference will run virtually in the period October 4-8.
- Number of registrations is not yet available.
- 8 tracks have been defined:
    - AMS, sensors and RF
    - VLSI circuits and SoC design
    - Embedded system design and software
    - CAD tools and methodologies for digital IC design and optimization
    - Verification, modelling and prototyping
    - Design for testability, reliability and fault tolerance

    - Hardware security
    - Emerging technologies and new computing paradigms
- Number of submissions: 75 (3/4 reviews per paper)
    - Main conference: 58
    - Special sessions: 8
    - PhD Forum: 9
- Accepted: 44
    - Main conference: 29 (19 for oral presentation, 10 posters)
    - Special session: 7
    - PhD Forum: 8

Track	Submissions	Accepted	Acceptance rate	PC members
Analog, Mixed Signal, Sensors and RF	6	3	50%	15
CAD Tools and Methodologies for Digital IC Design & Optimization	5	3	60%	14
Design for Testability, Reliability and Fault Tolerance	6	5	83%	15
Embedded Systems Design & Software	5	3	60%	14
Emerging Technologies and New Computing Paradigms	14	7	50%	15
Hardware Security	5	2	40%	17
Verification, Modeling and Prototyping	7	2	29%	12
VLSI Circuits and SoC Design	10	4	40%	21

- The program includes 3 keynotes and 3 industrial talks:
    - 3 keynotes
        - The Deep Learning Software Stack: What Every NN Accelerator Architect Should Know, Kurt Keutzer, UC Berkeley, USA
        - Preventing Secret leaks from Edge Devices, Ruby Lee, Princeton University, USA
        - Efficient Neuromorphic Chips With Emerging Circuits and Technologies, Damien Querlioz, CNRS, Université Paris-Saclay, France
    - 3 Industrial talks
        - Running Privacy-aware Machine Learning Applications on Edge Devices, Kaniskha Bhaduri, Apple, USA
        - Sunil Cheruvu, Intelligent Edge security challenges and HW based technologies to the rescue, Intel, USA
        - Optimizing memory device technology for energy efficient AI hardware, Peter Debacker, IMEC, Belgium
- The conference will be in the morning (European time). Graziano observes this can create problems to people from America. Anupam will investigate the possibility of moving the conference in the afternoon (European time).
- Ricardo highlights a misunderstanding for the PhD forum. The CFP reported about the presence of both a PhD and a student forum, but the submission website had only the

PhD Forum. The mistake was propagated from the last year. For the future this must be fixed by having two separate forums: one for PhDs and one for undergraduate students.

- During the opening ceremony there will be an introduction by Achim as TC 10 chair and the celebration of 40 years of VLSI-SOC with a presentation by Ricardo and Manfred. Approximately 45 mins for Ricardo and Manfred and 15 mins for Achim.

4. Status of VLSI-SOC 2022

Odysseas summarises the status of VLSI-SOC 2022 in Patras.

- Dates: October 3-5 2022
- Location: Cultural Centre of the University of Patras, hopefully not virtual
- Info about location and how to reach Patras are provided
- Negotiation with nearby hotels is ongoing for special rates
- Social events at either Olympia or Delphi
- Theme of the conference: SoCs for 5G Evolution and 6G
- Sponsors: IFIP, IEEE CEDA, ACM Sigda, IEEE CAS, University of Patras, Synopsys, MDPI
- Organizing committee: completed.

- Ricardo asks about the call for paper to include it in the next CASS magazine by November. Odysseas answers it will be available in September.
- Next plans are:
    - Signing the MOU
    - Contact with sponsors
    - Definition of budget
    - Preparation of the CFP
    - Publication of the VLSI-SOC 2022 web site

5. Status of VLSI-SOC 2023

No news at the moment. At the beginning of 2021, Said Hamdioui contacted some universities in Morocco. They are interested but only if COVID free.

6. Francois Anceau Workshops

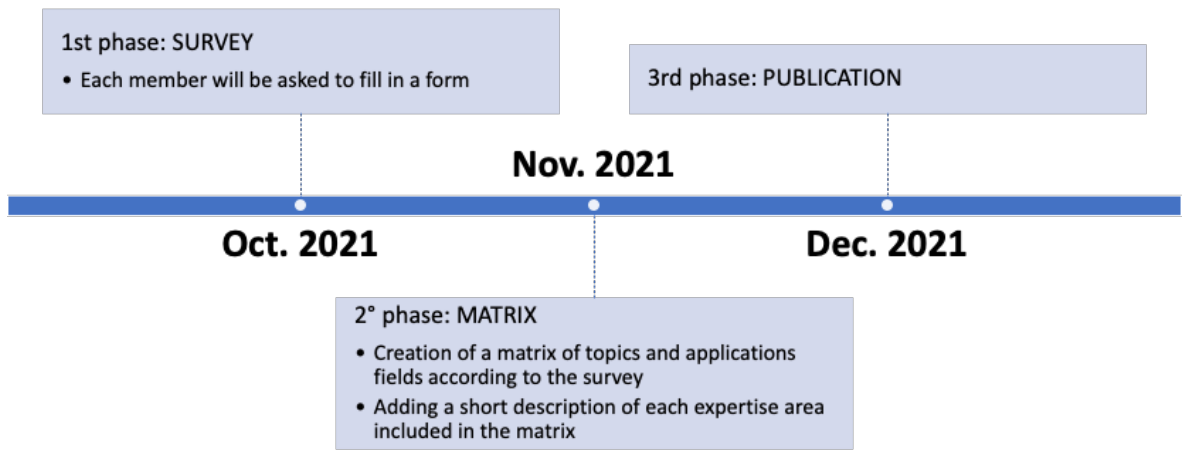
It is time to organize the workshop to promote it during VLSI-SOC 21 and the IFIP60 panel on Oct. 25.
Salvador remembers Ahmed proposed to have physical event in Grenoble. There will be a Winter school in January on formal languages in the 2nd week of January. The workshop could be scheduled at the beginning or end to the school, but how many people will attend?
Victor proposes to organize the event in hybrid form.
Then, Salvador proposes co-locate with FETCH workshop and having it hybrid.
Tiziana remembers that for some institution the physical participation is still not allowed, thus going hybrid is the best solution for now.
Salvador will talk with Ahmed for evaluating the different alternatives and he will update the WG in the next days.

7. Mapping of WG competences

Graziano remembers the idea of the mapping. The process has not started yet, but a discussion has been made in the past months with the WG vice-chairs to define the way of proceeding.
Tiziana summarizes the method she adopted in her department and that could be used also for the WG.

- Each member will be asked to fill in a form to create a mapping matrix with the following questions:
    - Name, surname, affiliation, position
    - VLSI-SOC topics they are interested in
    - Add more topics, if necessary
    - Up to 5 keywords representing the core technologies in the context of each flagged topic
    - Application domain per each flagged topic

The timeline will be probably as follows:



8. Any other business

Ricardo asks to talk about the Springer Book, which has been recently published. He remembers Fatih observed the papers from the Book are classified as conference proceedings in the Springer web site, while they are an extended version of them. This creates problem for the publication evaluation rankings, because conference proceedings have less value that book chapter in some rankings. Ricardo highlighted the problem to Springer. They answered this is due to their web site template and cannot be solved. After further pression by Ricardo, Springer decided to investigate how to solve the problem. Ricardo asks Achim to interact with IFIP to press Springer, such that the problem can be definitely solved.

Next meeting: to be defined.