IFIP Working Group 10.5 Minutes Meeting
International Congress Center Dresden
16/03/2015 (13:00-15:00)
In conjunction with DATE conference 2016

Notes taken by Masahiro Fujita and Dominique Borrione

Attendees: *David Atienza, Dominique Borrione, Kiyoung Choi, Masaharu Imai, Ian O'Connor, Michael Hübner, Luis Miguel Silveira, Donatella Sciuto, Salvador Mir, Fatih Ugurdad , Ayse Coskun, Masahiro Fujita*

Apologies*: Tiziana Margaria, Reiner Hartenstein, Takashi Kambe, Ahmed Jerraya, P.A. Subrahmanyam, Juergen Becker, Srinivas Katkoori, Chi Ying, Manfred Glesner, Ricardo Reis, Luc Claesen, Adam Pawlak, Flávio Rech Wagner, Alexander Stempkovsky, Ian O'Connor, Wolfgang Rosenstiel, Nikil Dutt*

Invited*: Maksim Jenihhin, Ibrahim Elfadel, Graziano Pravadelli*

Agenda

- Meeting in South Korea (VLSI-SoC): approval of minutes
- Status of preparation of VLSI-SoC 2016
- Status of preparation of VLSI-SoC 2017
- Applications for future venues of VLSI-SoC
- New member candidate
  - Prof. Graziano Pravadelli, University of Verona, Italy
  - Prof. Luciano Ost, University of Leicester, UK
- Others if any

Approval of minutes

The minutes have been approved without any changes.

Status of preparation of VLSI-SoC 2016 by Maksim Jenihhin, local arrangements chair

See attached slides. Information on slides is not repeated here.

The preparation of VLSI-SoC have been going generally well, but there is an issue whether we should go with financial sponsorships with IEEE as we did before or go with only technical

sponsorship with IEEE. The pros and cons were discussed. If we go only with technical sponsorship, we need to make sure that IEEE explore will surely have the papers. Also, the institution of the organizers must be insured in the case of loss in the conference. On the other hand, interactions/communications with IEEE can be reduced a lot if we go with technical sponsorship only. After discussions, Prof. Jenihhin said most likely VLSI-SoC 2016 will do the same with IEEE as before. If this is not the case, the steering committee of VLSI-SoC 2016 should contact WG10.5 immediately.

There are 91 persons and 10 tracks in the technical program committee.
The current submission deadlines are: April 18 for abstract and special sessions, April 25 for regular paper submission. This is the same deadline as ICCAD, and we should plan for a deadline extension that would allow VLSI-SOC to receive submissions that did not make it to ICCAD. There will be enough time left, since the review deadline is June 6.

The number of people we are expecting at Tallinn is 100 or more, which makes the conference budget safe. Plans are to collocate a workshop on September 29-30.
Discussion on the budget:

- The IFIP fee of 10€/day/participant has to be added to the expenditures.
- Plan 1000€ for delivery of the post conference Springer book.
- Show expectation of industry sponsorship and financial help, which would provide the amount needed to show the benefit required by IEEE.
- The budget for student travel is not yet in the budget calculation. Last year, TC 10 had provided funds to help students from developing countries.

Advance program outline:

- IFIP WG10.5 meeting: September 25, 14-16H.
- VLSI-SOC PC meeting: September 25, 16-18H. followed by a dinner
- Scientific program September 26-28. Two concurrent sessions. There will be both a reception on September 26, and a banquet on September 27.
- To be added in the program: one panel and one or more special sessions.

Status of preparation of VLSI-SoC 2017 by Ibrahim Elfadel

See attached slides. Information on slides is not repeated here.

The preparation is right in the track. There can be a good amount of governmental support (see the slides) with which the registration fee for the conference can be totally reduced. However, the initially proposed support of 250K AED (± 68K US$) from the Abu Dhabi Education Council might not be available any longer, due to the current low rate of oil. There were discussions how we should proceed, and several people indicated that free registration may not work well as we cannot accurately predict how many people will attend. So we decided to go with a normal registration fee, and governmental supports will be used to make the conference more attractive for students and others.

Currently the organizing committee is negotiating hotel rates. So far the quoted rate is a little bit high (see slides) compared to the previous conferences held in a hotel, and so there will be more negotiation on this issue. There are four less expensive hotels around the conference site.

At the request of Ibrahim Elfadel, in order to support the local faculty, there will be co-chairs for each position of responsibility in the VLSI-SOC'17 committee, with a local and an international co-chair person.

Applications for future venues of VLSI-SoC

Further contacts with Martin Margala must be done to see the possibility of organising VLSI-SoC'18 in the Boston area.

New member candidate

- **Prof. Graziano Pravadelli, University of Verona, Italy**

Prof. Pravadelli gave a short talk to introduce himself. He is a member of the EDS group at University of Verona, and co-founder of EDAlab in 2007. He has been working on verification issues on embedded systems and has developed various methods/tools, some of which have been commercialized. His main research interests are: ESL virtual prototyping, assertion-based verification (including assertion abstraction and reuse, assertion mining), high lelvl testing, TLM/RTL modeling, HW/SW co-simulation, modeling extra functional properties (power state machines).
Prof. Pravadelli expressed his intention to be an active group member, and possibly organize a future VLSI-SOC conference.

After the talk, everyone attendees has not doubt in this membership. Prof. Pravadelli is now a member of WG10.5.

- **Prof. Luciano Ost, University of Leicester, UK**

As he did not attend the meeting, discussions are postponed to the next meeting.

Next meeting: Austin, Texas, June 2016, in conjunction with DAC 2016