
Curriculum Vitae

of Enrico Fraccaroli

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Academic Profile

I am a postdoctoral research associate at the Department of Computer Science of the University of North Carolina at Chapel Hill (USA). My main research interests are the simulation of Networked Cyber-Physical Systems, focusing on analog components and automatic network synthesis.

My greatest achievement during my Ph.D. was the development of an innovative methodology for the abstraction of analog components inside Cyber-Physical Systems. This method can drastically reduce the overall simulation time of such systems so that they can be quickly verified, tested, and eventually re-engineered. While working on my thesis, I spent six months in a semiconductors supplier company called On Semiconductor in Belgium, under the supervision of Renaud Gillon. During this period, I improved and applied my methodology to real case studies obtaining great results. Right after this experience, I spent six months at the Pratt School of Engineering of Duke University, where I was supervised by Prof. Krishnendu Chakrabarty.

I obtained my Ph.D. in Computer Science in May 2019, supervised by Prof. Franco Fummi. Previously, I received my Master's and Bachelor's degrees from the University of Verona, respectively, in 2015 and 2012, after my Ph.D. I spent two years as a postdoc at the University of Verona before moving to my current position.

Research Statement

Analog abstraction : I started my research career, focusing on developing an efficient and reliable fault simulation methodology for Networked Cyber-Physical Systems (NCPSSs). During the first year of Ph.D., I developed the analog abstraction flow, a methodology that simplifies analog circuits and produces pure C/C++ code. I presented it for the first time at the conference DATE 2016 [C24], and then a more in-deep explanation in a journal paper at TCAD 2018 [J6]. I further expanded and improved the methodology and shown in several other conference publications [C23, C20] that the approach also works on other physical domains other than the electrical one, e.g., digital, mechanical, rotational. It also works with Micro Electro-Mechanical Systems (MEMSs), which are described with different physical domains.

Analog fault simulation : Then, I decided to apply the abstraction flow the functional safety field. I extended the abstraction flow for the automatic injection of faults and presented it at DATE [C21, C15], ASP-DAC [C22], ETS [C19], DCIS [C16], and FDL [C18, C17]. I also published a book chapter on the topic [B2]. The abstracted models were written in C++ and easily integrated with other simulation paradigms; as such, I moved to designs containing analog, digital, and network components. Once I could simulate all these heterogeneous components with high accuracy, I decided to perform fault injection inside NCPSSs.

Network synthesis and fault simulation : One of the critical parts of NCPSSs is communication; as such, I wanted to study a flow for the automatic generation of network infrastructures. The goal was to generate a network architecture optimized to reduce packet error rate, delay, power consumption, etc. The flow performs network synthesis and prepares a simulation infrastructure for injecting and simulating network faults. This branch of my work was presented in the journal paper TCOMP 2018 [J5]. I also published a book chapter on how to engineer Internet-of-Things (IoT) networks for Industry 4.0 [B1].

Holistic fault simulation : At the end of my Ph.D., I could generate a simulation environment written in C++ containing analog, digital, and network components and perform fault injection and simulation on them. I published a journal paper at TCOMP 2020 [J4]. At that time, the concept of Industry 4.0 was a few months old, and I decided to apply my expertise to the industrial domain. My objective was to master the simulation of production lines and also the automatic generation of network infrastructures of an industrial production plant. My research on the topic was published at DATE 2020 [C14] and 2021 [C12], ICPS 2021 [C10], and a recent journal paper at TETC 2021 [J3].

Transistor-level manipulation made open-source : In the last year of my Ph.D. I developed alongside my Ph.D. students *EDACurry*, an open-source tool for parsing, manipulating, and writing transistor-level descriptions. It supports different dialects (SPICE, Spectre, Eldo). The idea is to empower designers with a user-friendly tool for analyzing and editing those descriptions without relying on expensive commercial tools to do just one task (fault injection, conversion) or giving them no control. *EDACurry* was presented in a conference paper at FDL 2021 [C11].

Transistor-level defect modeling : I have recently been working with my Ph.D. students and a company to advance the state of the arts concerning “*Analog Defect Modeling and Coverage*”. We are developing improved fault simulation techniques and a list of advanced analog fault models that can better capture transistor-level defects. In a recent paper, we discussed our proposed techniques and models, compared them with the latest version of the draft standard IEEE P2427, and published the results at DDECS 2021 [C13].

Position History

Current Position

Date : 24/01/2022 – 23/01/2024
Position : Postdoctoral Research Associate,
Institution : Department of Computer Science, University of North Carolina at Chapel Hill, North Carolina, US,
Projects : Distributed embedded system design and optimization in the context of Industry 4.0;

Previous Positions

Date : 15/10/2019 – 31/12/2021
Position : Postdoctoral Research Fellow,
Institution : Department of Computer Science, University of Verona (Italy),
Projects : Hardware techniques for the automatic classification of data with functional safety characteristics;

Date : 15/10/2018 – 14/10/2019
Position : Postdoctoral Research Fellow,
Institution : Department of Computer Science, University of Verona (Italy),
Projects : Wearable IoT for FoG Prevention of Parkinson's Patients (BIPBIP);

Education

Date : 08/09/2015 – 14/05/2019, **PhD in Computer Science**,
Institution : Dept. of Computer Science, University of Verona - Italy,
Thesis : A Holistic Approach to Functional Safety for Networked Cyber-Physical Systems,
Advisor : Prof. Franco Fummi;

Date : 10/10/2012 – 19/03/2015, **Master's degree in Computer Science and Engineering**,
Institution : Dept. of Computer Science, University of Verona - Italy,
Thesis : Optimizing Virtual Platform Integration for Smart System Simulation,
Advisor : Prof. Davide Quaglia;

Date : 15/09/2008 – 21/03/2012, **Bachelor's degree in Computer Science**,
Institution : Dept. of Computer Science, University of Verona - Italy,
Thesis : Construction of a data warehouse to support screening of neonatal metabolic diseases,
Advisor : Prof. Carlo Combi;

Visiting Experiences

Date : 9/07/2018 – 8/12/2018
Institution : Pratt School of Engineering - Duke University
Supervisor : Prof. Krishnendu Chakrabarty
 This visit aimed at defining a methodology for abstracting transistor-level descriptions to behavioral-level (*i.e.*, from SPECTRE to Verilog-AMS).

Date : 06/12/2017 – 4/05/2018
Institution : ON Semiconductor B.V.B.A.
Supervisor : Renaud Gillon, PhD
 During this visit, I applied the abstraction methodology developed with Ph.D. in industrial descriptions written in SPICE and SPECTRE.

Awards and Recognitions

2021: Seal of Excellence. Certificate delivered by the European Commission for the project proposal “101062319, STRATEGic GUide to Smart manufacturing (STRATEGUS)”, submitted under the Horizon Europe Marie Skłodowska-Curie actions call HORIZON-MSCA-2021-PF-01-01 – MSCA Postdoctoral Fellowships 2021.

2020: Seal of Excellence. Certificate delivered by the European Commission for the project proposal “101025236, STRATEGic GUide to Smart manufacturing (STRATEGUS)”, submitted under the Horizon 2020's Marie Skłodowska-Curie actions call H2020-MSCA-IF-2020.

2018: Internationalization program scholarship (destination: Pratt School of Engineering - Duke University).

Teaching Activities

Position : **Contract Professor** of Computer Science (Laboratory),
Institution : Dept. of Electronics, Computer Science and Bioengineering, Politecnico di Milano (Italy),
Program : Bachelor's degree in Mechanical Engineering,
Acad. Years : 2019-20, 2020-21

Position : **Contract Professor** of Operating Systems (Laboratory),
Institution : Dept. of Computer Science, University of Verona (Italy),
Program : Bachelor's degree in Computer Science and Engineering,
Acad. Years : 2019-20

Position : **Instructor** of Design automation of embedded systems (Laboratory),
Institution : Dept. of Computer Science, University of Verona (Italy),
Program : Master's degree in Computer Science and Engineering,
Acad. Years : 2015-16, 2016-17

Position : **Instructor** of Introduction to computer architecture and operating systems (Laboratory),
Institution : Dept. of Computer Science, University of Verona (Italy),
Program : Master's degree in Computer Science and Engineering,
Acad. Years : 2015-16, 2016-17

Relevant Projects

The **project** is care the most, is the Mentoring OS (MentOS), an educational open source 32-bit linux-like Operating System that is currently used by the **University of Verona** for teaching **Operating Systems** classes. Its code as well as **ready-to-use lectures material** are **open-source**, and available online for everyone at mentos-team.github.io/. Both Prof. Tiziano Villa, and Prof. Graziano Pravadelli have used it for their classes 'Introduction to operating systems and networks' and 'Operating Systems', respectively.

Mentoring Activities

I co-advised: **6** Master's Students Thesis, **3** Bachelor's Students Thesis. I was a mentor to **8** younger Ph.D. students during my last year of Ph.D. and subsequent postdoctoral position.

Activities for the Scientific Community

Workshop Organizer

Organizer of the "National Workshop for Technology Transfer and Higher Education" for the Embedded Systems & Smart Manufacturing (ESSM) Laboratory of the National Interuniversity Consortium for Information Technology (CINI). A two days workshop that acted as a meeting place between industry and university researchers. [Click for more details.](#)

Session Chair

Session on "Intelligent and Flexible Manufacturing", at the IEEE 18th International Conference on Automation Science and Engineering (CASE), 2022. [Click for more details.](#)

Guest Editor

MDPI Special Issue "Design of Embedded Systems for Wireless Sensor Networks", 2021. [Click for more details.](#)

Special Session Chair

Special session on "Roles of Digital Twin in Industry 4.0", at the IEEE 25th International Conference on Emerging Technologies and Factory Automation (ETFFA), 2020. [Click for more details.](#)

Publication Chair

Publication chair for the ECSI/IEEE Forum on Design and Specification Languages (FDL), 2019. [Click for more details.](#)

Multimedia Chair

Multimedia chair for the ECSI/IEEE Forum on Design and Specification Languages (FDL), 2017. [Click for more details.](#)

Member of the Organizing Committee

Member of the organizing committee for the IEEE International Conference on Electromagnetics in Advanced Applications (ICEAA), 2017. [Click for more details.](#)

Technical Reviewer for peer-reviewed journals

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), IEEE Transactions on Computers (TCOMP), IEEE Transactions on Industrial Informatics (TII), MDPI Sensors

Technical Reviewer for peer-reviewed conferences

ACM/IEEE Design Automation Conference (DAC), IEEE Design, Automation & Test in Europe (DATE), IEEE/ACM International Conference On Computer Aided Design (ICCAD), IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), IEEE Forum for Specification and Design Languages (FDL), IEEE International Conference on Computer Design (ICCD), IEEE International Conference on Embedded Systems (VLSID), IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), IEEE International Workshop on Logic and Synthesis (IWLS), ACM/IEEE International Conference on Formal Methods and Models for System Design (MEMOCODE)

Most significant invited presentations

“*Network Synthesis for Industry 4.0*” IEEE/ACM Design, Automation And Test in Europe (DATE) 2019, Grenoble (France), March 9th, 2020.

“*Fault analysis in analog circuits through language manipulation and abstraction,*” Forum on Specification and Design Languages (FDL) 2017, Verona (Italy), September 18th, 2017.

“*A homogeneous framework for AMS languages instrumentation, abstraction and simulation,*” IEEE European Test Symposium (ETS) 2017, Limassol (Cyprus), May 22nd, 2017.

Publications

Book Chapters

[B1] **E. Fraccaroli** and D. Quaglia, “*Chapter 3: Engineering IoT Networks,*” in: F. Firouzi, K. Chakrabarty, S. Nassif (Eds.) “*Intelligent Internet of Things: From Device to Fog and Cloud.*” Springer International Publishing, due: December 14, 2019, doi: [10.1007/978-3-030-30367-9](https://doi.org/10.1007/978-3-030-30367-9).

[B2] **E. Fraccaroli**, F. Stefanni, F. Fummi and M. Zwolinski, “*Fault analysis in analog circuits through language manipulation and abstraction,*” in: D. Große, S. Vinco, H. Patel (Eds.) “*Lecture Notes in Electrical Engineering.*” Springer International Publishing, December 20, 2018, doi: [10.1007/978-3-030-02215-0_5](https://doi.org/10.1007/978-3-030-02215-0_5).

Journal publications

[J1] S. Azam, N. Dall’Ora, **E. Fraccaroli**, R. Gillon and F. Fummi, “*Analog Defect Injection and Fault Simulation Techniques: A Systematic Literature Review,*” in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, doi: [10.1109/TCAD.2023.3298698](https://doi.org/10.1109/TCAD.2023.3298698).

[J2] **E. Fraccaroli** and S. Vinco, “*Modeling Cyber-Physical Production Systems with SystemC-AMS,*” in IEEE Transactions on Computers, vol. 72, no. 7, pp. 2039-2051, 1 July 2023, doi: [10.1109/TC.2022.3226567](https://doi.org/10.1109/TC.2022.3226567).

[J3] N. Dall’Ora, K. Alamin, **E. Fraccaroli**, M. Poncino, D. Quaglia and S. Vinco, “*Digital Transformation of a Production Line: Network Design, Online Data Collection and Energy Monitoring,*” in IEEE Transactions on Emerging Topics in Computing, vol. 10, no. 1, pp. 46-59, 1 Jan.-March 2022, doi: [10.1109/TETC.2021.3132432](https://doi.org/10.1109/TETC.2021.3132432).

[J4] **E. Fraccaroli**, M. Lora, and F. Fummi, “*Automatic Generation of Analog/Mixed Signal Virtual Platforms for Smart Systems,*” in IEEE Transactions on Computers, vol. 69, no. 9, pp. 1263-1278, 1 Sept. 2020, doi: [10.1109/TC.2020.2970699](https://doi.org/10.1109/TC.2020.2970699).

[J5] **E. Fraccaroli**, F. Stefanni, R. Rizzi, D. Quaglia and F. Fummi, “*Network Synthesis for Distributed Embedded Systems,*” in IEEE Transactions on Computers, vol. 67, no. 9, pp. 1315-1330, 1 Sept. 2018, doi: [10.1109/TC.2018.2812797](https://doi.org/10.1109/TC.2018.2812797).

[J6] M. Lora, S. Vinco, **E. Fraccaroli**, D. Quaglia and F. Fummi, “*Analog Models Manipulation for Effective Integration in Smart System Virtual Platforms,*” in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 37, no. 2, pp. 378-391, Feb. 2018, doi: [10.1109/TCAD.2017.2705129](https://doi.org/10.1109/TCAD.2017.2705129).

Conference publications

[C1] Nicola Dall’Ora, Sadia Azam, **Enrico Fraccaroli**, Renaud Gillon and Franco Fummi, “*Verilog-A Implementation of Generic Defect Templates for Analog Fault Injection,*” in Proceedings of the Great Lakes Symposium on VLSI 2023 (GLSVLSI ’23). Association for Computing Machinery, New York, NY, USA, 477–481, doi: [10.1145/3583781.3590317](https://doi.org/10.1145/3583781.3590317)

[C2] **E. Fraccaroli**, P. Joshi, S. Xu, K. Shazzad, M. Jochim and S. Chakraborty, “*Timing Predictability for SOME/IP-based Service-Oriented Automotive In-Vehicle Networks,*” 2023 Design, Automation & Test in Europe Conference & Exhibition (DATE), Antwerp, Belgium, 2023, pp. 1-6, doi: [10.23919/DATE56975.2023.10137065](https://doi.org/10.23919/DATE56975.2023.10137065).

- [C3] F. Tosoni, N. Dall’Ora, **E. Fraccaroli** and F. Fummi, “*A Framework for Modeling and Concurrently Simulating Mechanical and Electrical Faults in Verilog-AMS*,” 2022 Forum on Specification & Design Languages (FDL), Linz, Austria, 2022, pp. 1–8, doi: [10.1109/FDL56239.2022.9925655](https://doi.org/10.1109/FDL56239.2022.9925655).
- [C4] M. Balszun, C. Hobbs, **E. Fraccaroli**, D. Roy and S. Chakraborty, “*Exploiting Process Dynamics in Multi-Stage Schedule Optimization for Flexible Manufacturing*,” 2022 IEEE 27th International Conference on Emerging Technologies and Factory Automation (ETFA), 2022, pp. 1–8, doi: [10.1109/ETFA52439.2022.9921465](https://doi.org/10.1109/ETFA52439.2022.9921465).
- [C5] F. Tosoni, N. Dall’Ora, **E. Fraccaroli** and F. Fummi, “*The Challenges of Coupling Digital-Twins with Multiple Classes of Faults*,” 2022 IEEE 23rd Latin American Test Symposium (LATS), Montevideo, Uruguay, 2022, pp. 1–6, doi: [10.1109/LATS57337.2022.9937026](https://doi.org/10.1109/LATS57337.2022.9937026).
- [C6] M. Balszun, C. Hobbs, **E. Fraccaroli**, D. Roy, F. Fummi and S. Chakraborty, “*Process Dynamics-Aware Flexible Manufacturing for Industry 4.0*,” 2022 IEEE 18th International Conference on Automation Science and Engineering (CASE), 2022, pp. 2375–2382, doi: [10.1109/CASE49997.2022.9926495](https://doi.org/10.1109/CASE49997.2022.9926495).
- [C7] S. Azam, N. Dall’Ora, **E. Fraccaroli**, A. Alberts, R. Gillon and F. Fummi, “*Investigation on Realistic Stuck-on/off Defects to Complement IEEE P2427 Draft Standard*,” 23rd International Symposium on Quality Electronic Design (ISQED), 2022, pp. 51–57, doi: [10.1109/ISQED54688.2022.9806269](https://doi.org/10.1109/ISQED54688.2022.9806269).
- [C8] N. Dall’Ora, F. Tosoni, **E. Fraccaroli** and F. Fummi, “*Inferring Mechanical Fault Models from the Electrical Domain*,” IEEE 5th International Conference on Industrial Cyber-Physical Systems (ICPS), 2022, pp. 01–08, doi: [10.1109/ICPS51978.2022.9817009](https://doi.org/10.1109/ICPS51978.2022.9817009).
- [C9] S. Azam, N. Dall’Ora, **E. Fraccaroli** and F. Fummi, “*Functional Level Abstraction and Simulation of Verilog-AMS Piecewise Linear Models*,” 23rd International Symposium on Quality Electronic Design (ISQED), 2022, pp. 39–44, doi: [10.1109/ISQED54688.2022.9806273](https://doi.org/10.1109/ISQED54688.2022.9806273).
- [C10] N. Dall’Ora, **E. Fraccaroli**, S. Vinco and F. Fummi, “*Multi-Discipline Fault Modeling with Verilog-AMS*,” 2021 4th IEEE International Conference on Industrial Cyber-Physical Systems (ICPS), 2021, pp. 237–243, doi: [10.1109/ICPS49255.2021.9468133](https://doi.org/10.1109/ICPS49255.2021.9468133).
- [C11] N. Dall’Ora, S. Azam, **E. Fraccaroli**, A. Alberts and F. Fummi, “*A Common Manipulation Framework for Transistor-Level Languages*,” 2021 Forum on specification & Design Languages (FDL), 2021, pp. 01–07, doi: [10.1109/FDL53530.2021.9568379](https://doi.org/10.1109/FDL53530.2021.9568379).
- [C12] K. Alamin, S. Vinco, M. Poncino, N. Dall’Ora, **E. Fraccaroli** and D. Quaglia, “*Digital Twin Extension with Extra-Functional Properties*,” 2021 Design, Automation & Test in Europe Conference & Exhibition (DATE), 2021, pp. 434–439, doi: [10.23919/DATE51398.2021.9474220](https://doi.org/10.23919/DATE51398.2021.9474220).
- [C13] N. Dall’Ora, S. Azam, **E. Fraccaroli**, A. Alberts and F. Fummi, “*Predictive Fault Grouping based on Faulty AC Matrices*,” 2021 24th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), 2021, pp. 11–16, doi: [10.1109/DDECS52668.2021.9417072](https://doi.org/10.1109/DDECS52668.2021.9417072).
- [C14] **E. Fraccaroli**, A. M. Padovani, D. Quaglia and F. Fummi, “*Network Synthesis for Industry 4.0*,” 2020 Design, Automation & Test in Europe Conference & Exhibition (DATE), Grenoble, France, 2020, pp. 1692–1697, doi: [10.23919/DATE48585.2020.9116407](https://doi.org/10.23919/DATE48585.2020.9116407).
- [C15] S. Centomo, **E. Fraccaroli** and M. Panato, “*From Multi-Level to Abstract-Based Simulation of a Production Line*,” 2019 Design, Automation & Test in Europe Conference & Exhibition (DATE), Florence, Italy, 2019, pp. 1253–1256, doi: [10.23919/DATE.2019.8714870](https://doi.org/10.23919/DATE.2019.8714870).
- [C16] **E. Fraccaroli**, D. Quaglia and F. Fummi, “*Efficient Simulation of Faults in Networked Cyber-Physical Systems*,” 2018 Conference on Design of Circuits and Integrated Systems (DCIS), Lyon, France, 2018, pp. 1–6, doi: [10.1109/DCIS.2018.8681483](https://doi.org/10.1109/DCIS.2018.8681483).
- [C17] **E. Fraccaroli**, D. Quaglia and F. Fummi, “*Simulation-based Holistic Functional Safety Assessment for Networked Cyber-Physical Systems*,” 2018 Forum on specification & Design Languages (FDL), Garching, 2018, pp. 5–16, doi: [10.1109/FDL.2018.8524050](https://doi.org/10.1109/FDL.2018.8524050).
- [C18] **E. Fraccaroli**, F. Stefanni, F. Fummi and M. Zwolinski, “*Fault analysis in analog circuits through language manipulation and abstraction*,” 2017 Forum on specification & Design Languages (FDL), Verona, 2017, pp. 1–7, doi: [10.1109/FDL.2017.8303890](https://doi.org/10.1109/FDL.2017.8303890).
- [C19] **E. Fraccaroli**, L. Piccolboni and F. Fummi, “*A homogeneous framework for AMS languages instrumentation, abstraction and simulation*,” 2017 22nd IEEE European Test Symposium (ETS), Limassol, 2017, pp. 1–2, doi: [10.1109/ETS.2017.7968212](https://doi.org/10.1109/ETS.2017.7968212).
- [C20] **E. Fraccaroli**, M. Lora and F. Fummi, “*Automatic abstraction of multi-discipline analog models for efficient functional simulation*,” Design, Automation & Test in Europe Conference & Exhibition (DATE), 2017, Lausanne, 2017, pp. 662–665, doi: [10.23919/DATE.2017.7927072](https://doi.org/10.23919/DATE.2017.7927072).
- [C21] **E. Fraccaroli** and F. Fummi, “*Analog fault testing through abstraction*,” Design, Automation & Test in Europe Conference & Exhibition (DATE), 2017, Lausanne, 2017, pp. 270–273, doi: [10.23919/DATE.2017.7926996](https://doi.org/10.23919/DATE.2017.7926996).
- [C22] M. Lora, **E. Fraccaroli** and F. Fummi, “*Virtual prototyping of smart systems through automatic abstraction and mixed-signal scheduling*,” 2017 22nd Asia and South Pacific Design Automation Conference (ASP-DAC), Chiba, 2017, pp. 232–237, doi: [10.1109/ASPDAC.2017.7858325](https://doi.org/10.1109/ASPDAC.2017.7858325).

- [C23] **E. Fraccaroli**, M. Lora, F. Fummi and P. Montuschi, “*A fast simulation environment for smart systems validation in presence of electromagnetic interferences,*” 2016 International Conference on Electromagnetics in Advanced Applications (ICEAA), Cairns, QLD, 2016, pp. 740–743, doi: [10.1109/ICEAA.2016.7731505](https://doi.org/10.1109/ICEAA.2016.7731505).
- [C24] **E. Fraccaroli**, M. Lora, S. Vinco, D. Quaglia and F. Fummi, “*Integration of mixed-signal components into virtual platforms for holistic simulation of smart systems,*” 2016 Design, Automation & Test in Europe Conference & Exhibition (DATE), Dresden, 2016, pp. 1586–1591, doi: [10.3850/9783981537079_0376](https://doi.org/10.3850/9783981537079_0376).
- [C25] C. Barnes, J. Cottin, D. Quaglia, **E. Fraccaroli**, A. Pegatoquet, F. Verdier, S. Angeleri, “*Network-Aware Virtual Platform for the Verification of Embedded Software for Communications,*” 2015 Euromicro Conference on Digital System Design, Funchal, 2015, pp. 518–525, doi: [10.1109/DSD.2015.110](https://doi.org/10.1109/DSD.2015.110).

In compliance with the GDPR regulation (EU) 2016/679, and the Italian Legislative Decree no. 196 dated 30/06/2003, I hereby authorize you to use and process my personal details.

Chapel Hill, August 3, 2023



Enrico Fraccaroli